FAIRCHILD SEMICONDUCTOR®

September 2007

FSQ0365, FSQ0265, FSQ0165, FSQ321, FSQ311 Green Mode Fairchild Power Switch (FPS™) for Valley Switching Converter - Low EMI and High Efficiency

Features

- Optimized for Valley Switching (VSC)
- Low EMI through Variable Frequency Control and Inherent Frequency Modulation
- High-Efficiency through Minimum Voltage Switching
- Narrow Frequency Variation Range over Wide Load and Input Voltage Variation
- Advanced Burst-Mode Operation for Low Standby Power Consumption
- Pulse-by-Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD)
- Under-Voltage Lockout (UVLO) with Hysteresis
- Internal Start-up Circuit
- Internal High-Voltage SenseFET (650V)
- Built-in Soft-Start (15ms)

Applications

- Power Supply for DVP Player and DVD Recorder, Set-Top Box
- Adapter
- Auxiliary Power Supply for PC, LCD TV, and PDP TV

Related Application Notes

- AN-4137, AN-4141, AN-4147, AN-4150 (Flyback)
- AN-4134 (Forward)

Description

A Valley Switching Converter generally shows lower EMI and higher power conversion efficiency than a conventional hard-switched converter with a fixed switching frequency. The FSQ-series is an integrated Pulse-Width Modulation (PWM) controller and SenseFET specifically designed for valley switching operation with minimal external components. The PWM controller includes an integrated fixed-frequency oscillator, Under-Voltage Lockout, Leading Edge Blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise current sources for loop compensation, and self-protection circuitry.

Compared with discrete MOSFET and PWM controller solutions, the FSQ-series reduces total cost, component count, size and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform that is well suited for cost-effective designs of valley switching fly-back converters.

FPS™ is a trademark of Fairchild Semiconductor Corporation.

Ordering Information

Product Number[5]	PKG.	Operating Temp.	Current Limit	$R_{DS(ON)}$ Max.	Maximum Output Power[1]				Replaces Devices
					230VAC±15%[2]		85-265VAC		
					Adapter[3]	Open-Frame[4]	Adapter[3]	Open-Frame[4]	
FSQ311	8-DIP	-40 to +85C	0.6A	19Ω	7W	10W	6W	8W	FSDL321 FSDM311
FSQ311L	8-LSOP								
FSQ321	8-DIP	-40 to +85°C	0.6A	19Ω	8W	12W	7W	10W	FSDL321 FSDM311
FSQ321L	8-LSOP								
FSQ0165RN	8-DIP	-40 to +85°C	0.9A	10Ω	10W	15W	9W	13W	FSDL0165RN
FSQ0165RL	8-LSOP								
FSQ0265RN	8-DIP	-40 to +85°C	1.2A	6Ω	14W	20W	11W	16W	FSDM0265RN FSDM0265RNB
FSQ0265RL	8-LSOP								
FSQ0365RN	8-DIP	-40 to +85°C	1.5A	4.5Ω	17.5W	25W	13W	19W	FSDM0365RN FSDM0365RNB
FSQ0365RL	8-LSOP								

Notes:
1. The junction temperature can limit the maximum output power.
2. $230V_{AC}$ or $100/115V_{AC}$ with doubler. The maximum power with CCM operation.
3. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
4. Maximum practical continuous power in an open-frame design at 50°C ambient.
5. Pb-free package per JEDEC J-STD-020B.

Typical Circuit

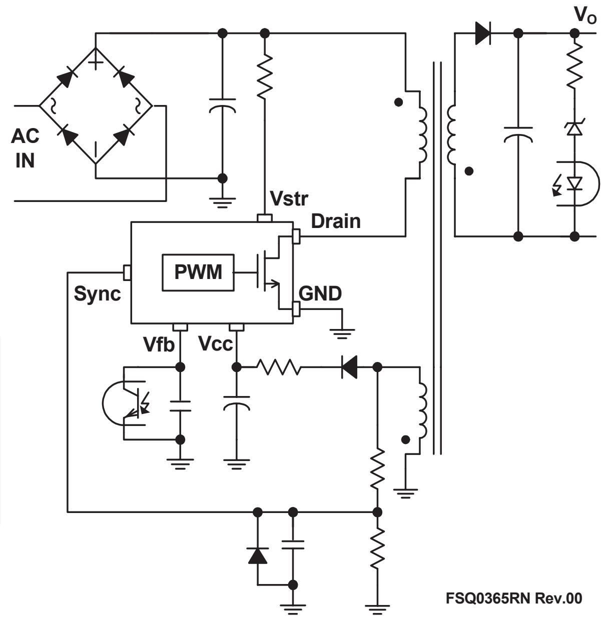

Figure 1. Typical Flyback Application

Internal Block Diagram

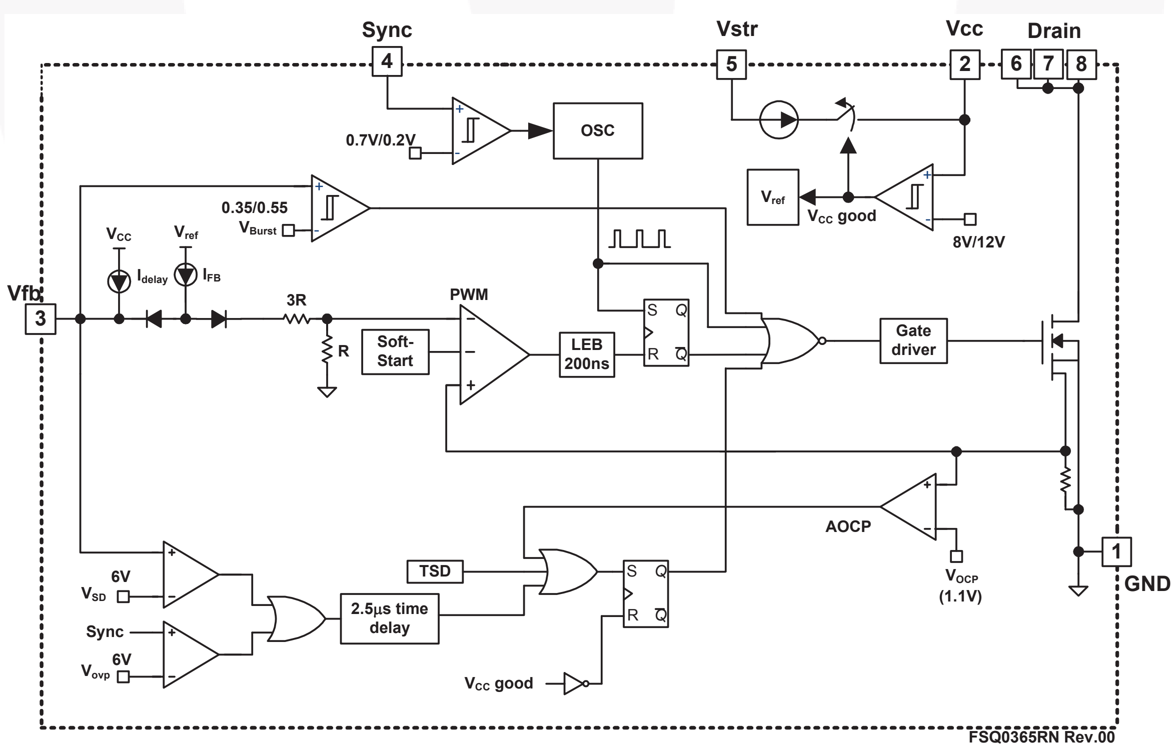

Figure 2. Functional Block Diagram

Pin Configuration

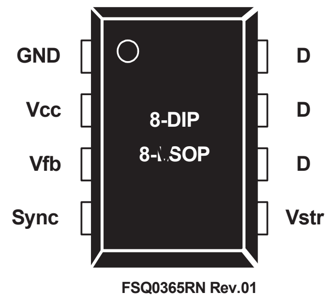

Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	SenseFET source terminal on primary side and internal control ground.
2	Vcc	Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (see Internal Block Diagram Section). It is not until V_{CC} reaches the UVLO upper threshold (12V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	Vfb	The feedback voltage pin is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally while a capacitor and optocoupler are typically connected externally. There is a time delay while charging external capacitor Cfb from 3V to 6V using an internal 5μA current source. This time delay prevents false triggering under transient conditions but still allows the protection mechanism to operate under true overload conditions.
4	Sync	This pin is internally connected to the sync-detect comparator for valley switching. Typically the voltage of the auxiliary winding is used as Sync input voltage and external resistors and capacitor are needed to make time delay to match valley point. The threshold of the internal sync comparator is 0.7V/0.2V.
5	Vstr	This pin is connected to the rectified AC line voltage source. At start-up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 12V, the internal switch is opened.
6,7,8	Drain	The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 700V. Minimizing the length of the trace connecting these pins to the transformer will decrease leakage inductance.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25°C, unless otherwise specified.

Symbol	Characteristic		Min.	Max.	Unit
V_{STR}	V_{str} Pin Voltage		500		V
V_{DS}	Drain Pin Voltage		650		V
V_{CC}	Supply Voltage			20	V
V_{FB}	Feedback Voltage Range		-0.3	9.0	V
V_{Sync}	Sync Pin Voltage Range		-0.3	9.0	V
I_{DM}	Drain Current Pulsed(6)	FSQ0365		12	A
		FSQ0265		8	
		FSQ0165		4	
		FSQ321/311		1.5	
E_{AS}	Single Pulsed Avalanche Energy(7)	FSQ0365		230	mJ
		FSQ0265		140	
		FSQ0165		50	
		FSQ321/311		10	
P_D	Total Power Dissipation			1.5	W
T_J	Recommended Operating Junction Temperature		-40	Internally limited	°C
T_A	Operating Ambient Temperature		-40	85	°C
T_{STG}	Storage Temperature		-55	150	°C
ESD	Human Body Model(8)		CLASS1 C		
	Machine Model(8)		CLASS B		

Notes:
6. Repetitive rating: Pulse width limited by maximum junction temperature.
7. L=51mH, starting T_J=25°C.
8. Meets JEDEC standards JESD22-A114 and JESD22-A115.

Thermal Impedance

Symbol	Parameter	Value	Unit
8-DIP(9)			
θ_{JA}(10)	Junction-to-Ambient Thermal Resistance	80	°C/W
θ_{JC}(11)	Junction-to-Case Thermal Resistance	20	
θ_{JT}(12)	Junction-to-Top Thermal Resistance	35	

Notes:
9. All items are tested with the standards JESD 51-2 and 51-10 (DIP).
10. Free-standing, with no heat-sink, under natural convection.
11. Infinite cooling condition - refer to the SEMI G30-88.
12. Measured on the package top surface.

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
SenseFET Section							
BV_{DSS}	Drain Source Breakdown Voltage		V_{CC} = 0V, I_D = 100µA	650			V
I_{DSS}	Zero-Gate-Voltage Drain Current		V_{DS} = 560V			100	µA
$R_{DS(ON)}$	Drain-Source On-State Resistance(13)	FSQ0365	T_J = 25°C, I_D = 0.5A		3.5	4.5	Ω
		FSQ0265			5.0	6.0	
		FSQ0165			8.0	10.0	
		FSQ321/311			14.0	19.0	
C_{SS}	Input Capacitance	FSQ0365	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		315		pF
		FSQ0265			550		
		FSQ0165			250		
		FSQ321/311			162		
C_{OSS}	Output Capacitance	FSQ0365	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		47		pF
		FSQ0265			38		
		FSQ0165			25		
		FSQ321/311			18		
C_{RSS}	Reverse Transfer Capacitance	FSQ0365	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		9.0		pF
		FSQ0265			17.0		
		FSQ0165			10.0		
		FSQ321/311			3.8		
$t_{d(on)}$	Turn-On Delay Time	FSQ0365	V_{DD} = 350V, I_D = 25mA		11.2		ns
		FSQ0265			20.0		
		FSQ0165			12.0		
		FSQ321/311			9.5		
t_r	Rise Time	FSQ0365	V_{DD} = 350V, I_D = 25mA		34		ns
		FSQ0265			15		
		FSQ0165			4		
		FSQ321/311			19		
$t_{d(off)}$	Turn-Off Delay Time	FSQ0365	V_{DD} = 350V, I_D = 25mA		28.2		ns
		FSQ0265			55.0		
		FSQ0165			30.0		
		FSQ321/311			33.0		
t_f	Fall Time	FSQ0365	V_{DD} = 350V, I_D = 25mA		32		ns
		FSQ0265			25		
		FSQ0165			10		
		FSQ321/311			42		
Control Section							
$t_{ON.MAX1}$	Maximum On Time1	All but Q321	T_J = 25°C	10.5	12.0	13.5	µs
$t_{ON.MAX2}$	Maximum On Time2	Q321	T_J = 25°C	6.35	7.06	7.77	µs
t_{B1}	Blanking Time1	All but Q321		13.2	15.0	16.8	µs
t_{B2}	Blanking Time2	Q321		7.5	8.2		µs

Electrical Characteristics (Continued)

T_A = 25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
t_W	Detection Time Window		T_J = 25°C, V_{sync} = 0V		3.0		µs
f_{S1}	Initial Switching Freq.1	All but Q321		50.5	55.6	61.7	kHz
f_{S2}	Initial Switching Freq.2	Q321		84.0	89.3	95.2	kHz
Δf_S	Switching Frequency Variation(14)		-25°C < T_J < 85°C		±5	±10	%
I_{FB}	Feedback Source Current		V_{FB} = 0V	700	900	1100	µA
D_{MIN}	Minimum Duty Cycle		V_{FB} = 0V			0	%
V_{START}	UVLO Threshold Voltage		After turn-on	11	12	13	V
V_{STOP}				7	8	9	V
$t_{S/S1}$	Internal Soft-Start Time1	All but Q321	With free-running frequency		15		ms
$t_{S/S2}$	Internal Soft-Start Time2	Q321	With free-running frequency		10		ms
Burst Mode Section							
V_{BURH}	Burst-Mode Voltage		T_J = 25°C, t_{PD} = 200ns(15)	0.45	0.55	0.65	V
V_{BURL}				0.25	0.35	0.45	V
$V_{BUR(HYS)}$					200		mV
Protection Section							
I_{LIM}	Peak Current Limit	FSQ0365	T_J = 25°C, di/dt = 240mA/µs	1.32	1.50	1.68	A
		FSQ0265	T_J = 25°C, di/dt = 200mA/µs	1.06	1.20	1.34	
		FSQ0165	T_J = 25°C, di/dt = 175mA/µs	0.8	0.9	1.0	
		FSQ321	T_J = 25°C, di/dt = 125mA/µs	0.53	0.60	0.67	
		FSQ311	T_J = 25°C, di/dt = 112mA/µs	0.53	0.60	0.67	
V_{SD}	Shutdown Feedback Voltage		V_{CC} = 15V	5.5	6.0	6.5	V
I_{DELAY}	Shutdown Delay Current		V_{FB} = 5V	4	5	6	µA
t_{LEB}	Leading-Edge Blanking Time(14)				200		ns
V_{OVP}	Over-Voltage Protection		V_{CC} = 15V, V_{FB} = 2V	5.5	6.0	6.5	V
t_{OVP}	Over-Voltage Protection Blanking Time			2	3	4	µs
T_{SD}	Thermal Shutdown Temperature(14)			125	140	155	°C
Sync Section							
V_{SH}	Sync Threshold Voltage			0.55	0.70	0.85	V
V_{SL}				0.14	0.20	0.26	V
t_{Sync}	Sync Delay Time(14)(16)				300		ns
Total Device Section							
I_{OP}	Oper. Supply Current (Control Part Only)		V_{CC} = 15V	1	3	5	mA
I_{START}	Start Current		V_{CC} = V_{START} - 0.1V (before V_{CC} reaches V_{START})	270	360	450	µA
I_{CH}	Start-up Charging Current		V_{CC} = 0V, V_{STR} = min. 40V	0.65	0.85	1.00	mA
V_{STR}	Minimum V_{STR} Supply Voltage				26		V

Notes:

13. Pulse test: Pulse-Width=300µs, duty=2%
14. Though guaranteed, it is not 100% tested in production.
15. Propagation delay in the control IC.
16. Includes gate turn-on time.

Comparison Between FSDM0x65RNB and FSQ-Series

Function	FSDM0x65RNB	FSQ-Series	FSQ-Series Advantages
Operation method	Constant frequency PWM	Valley switching operation	■ Improved efficiency by valley switching ■ Reduced EMI noise
EMI reduction	Frequency modulation	Valley switching & inherent frequency modulation	■ Reduce EMI noise by two ways
Burst-mode operation	Fixed burst peak	Advanced burst-mode	■ Improved standby power by valley switching also in burst-mode ■ Because the current peak during burst operation is dependent on V_{FB}, it is easier to solve audible noise
Protection		AOCP	■ Improved reliability through precise abnormal over-current protection

Typical Performance Characteristics

These characteristic graphs are normalized at T_A= 25°C.

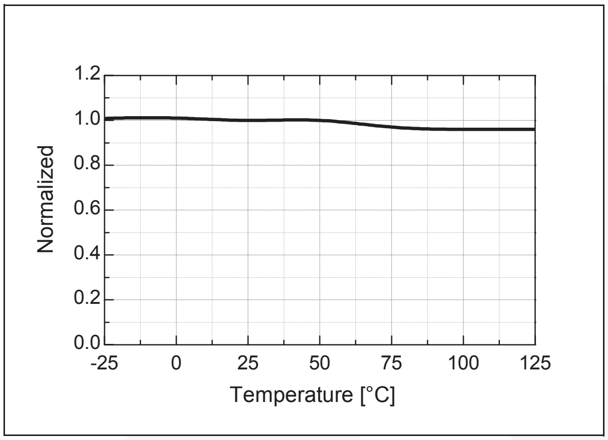

Figure 4. Operating Supply Current (I_{OP}) vs. T_A

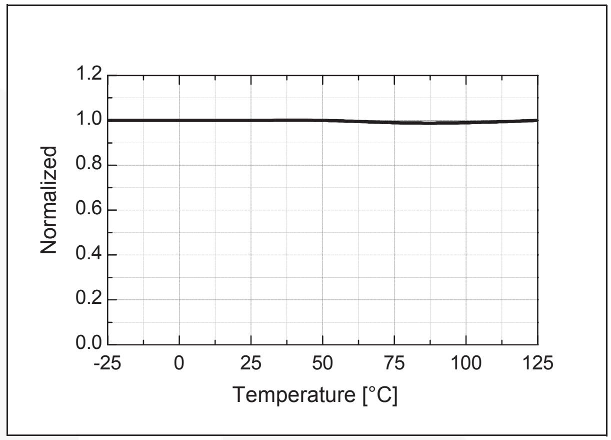

Figure 5. UVLO Start Threshold Voltage (V_{START}) vs. T_A

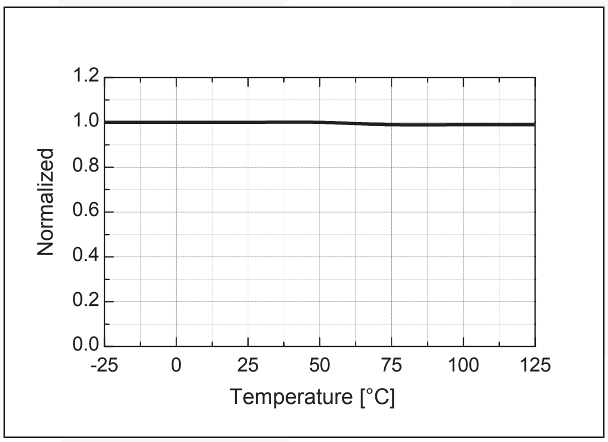

Figure 6. UVLO Stop Threshold Voltage (V_{STOP}) vs. T_A

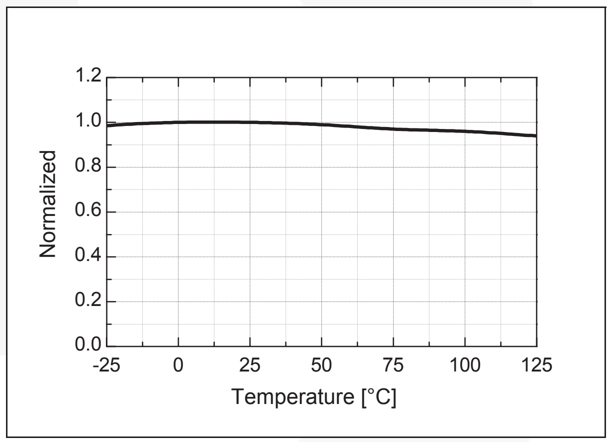

Figure 7. Start-up Charging Current (I_{CH}) vs. T_A

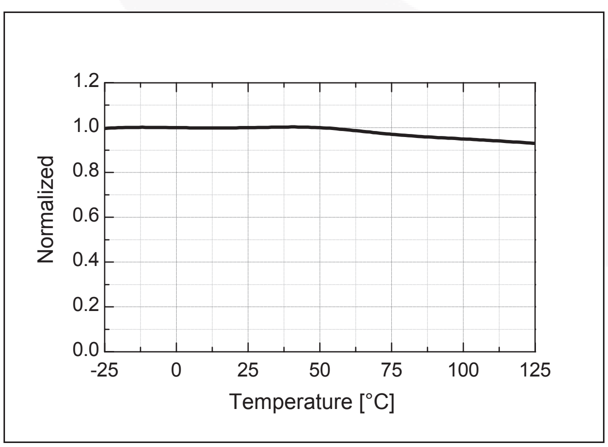

Figure 8. Initial Switching Frequency (f_S) vs. T_A

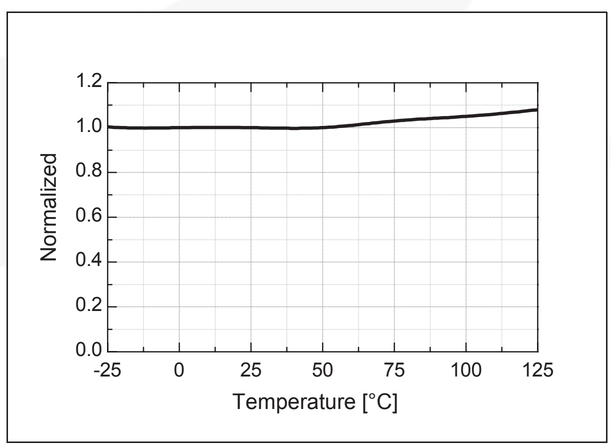

Figure 9. Maximum On Time ($t_{ON.MAX}$) vs. T_A

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A= 25°C.

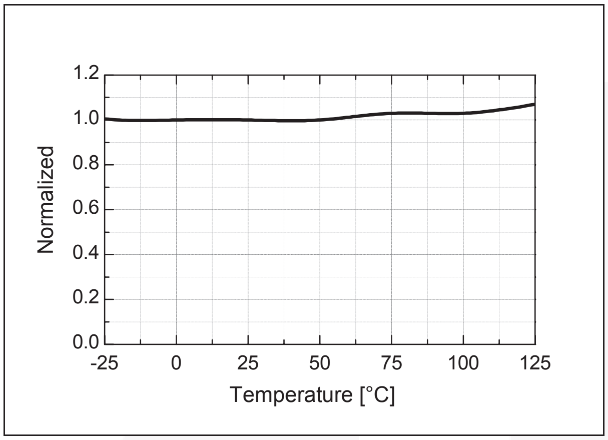

Figure 10. Blanking Time (t_B) vs. T_A

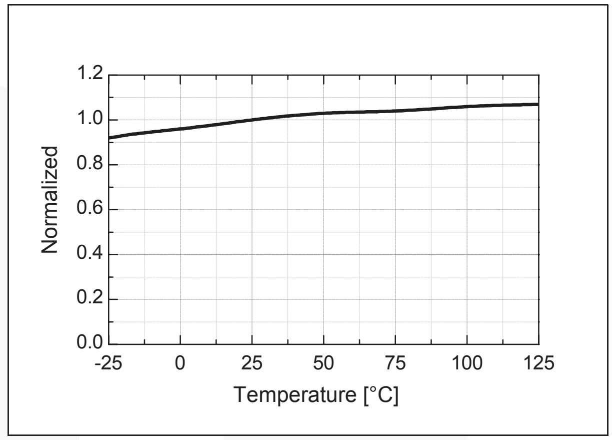

Figure 11. Feedback Source Current (I_{FB}) vs. T_A

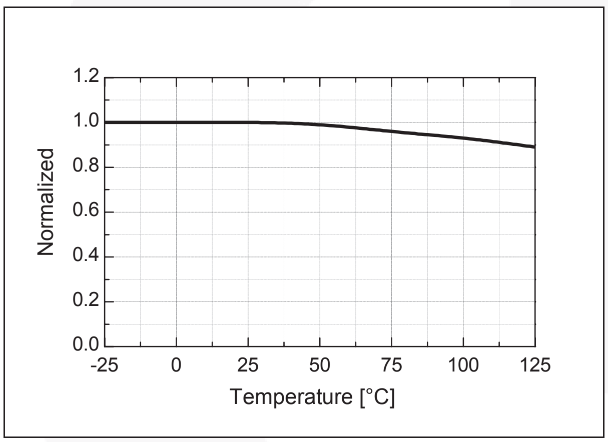

Figure 12. Shutdown Delay Current (I_{DELAY}) vs. T_A

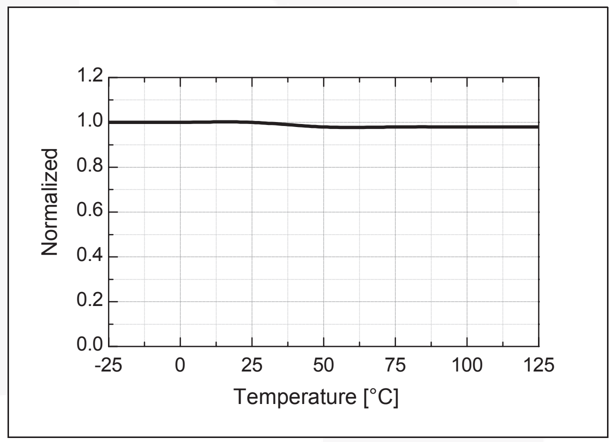

Figure 13. Burst-Mode High Threshold Voltage (V_{burh}) vs. T_A

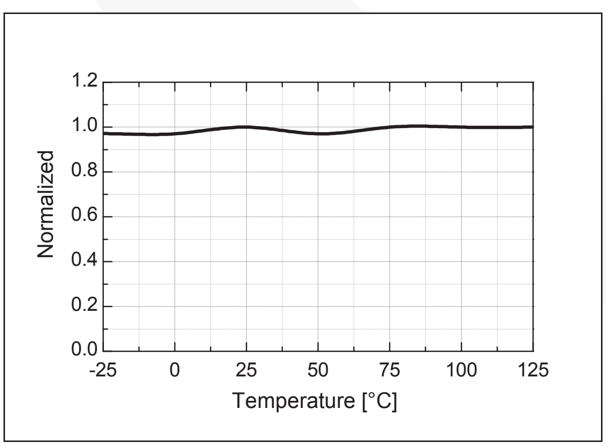

Figure 14. Burst-Mode Low Threshold Voltage (V_{burl}) vs. T_A

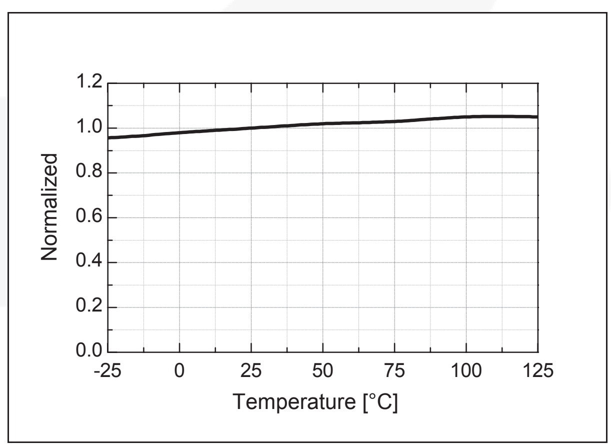

Figure 15. Peak Current Limit (I_{LIM}) vs. T_A

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A= 25°C.

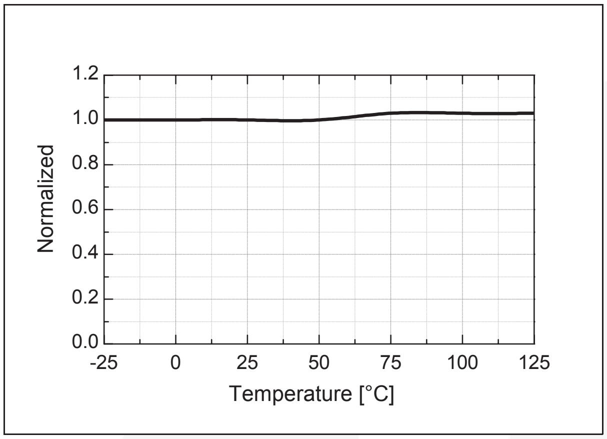

Figure 16. Sync High Threshold Voltage (V_{SH}) vs. T_A

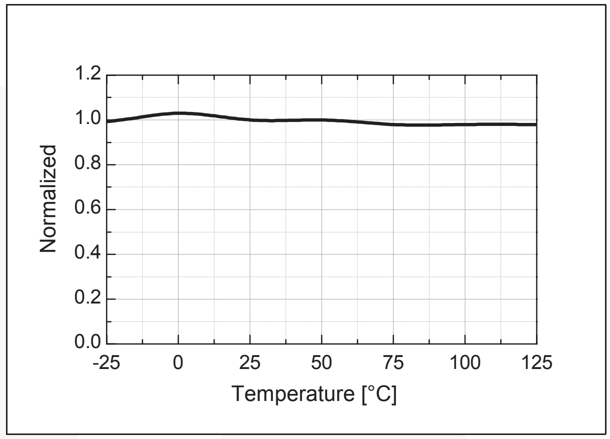

Figure 17. Sync Low Threshold Voltage (V_{SL}) vs. T_A

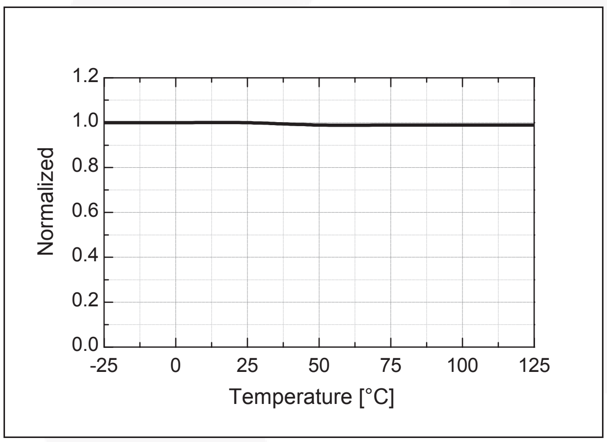

Figure 18. Shutdown Feedback Voltage (V_{SD}) vs. T_A

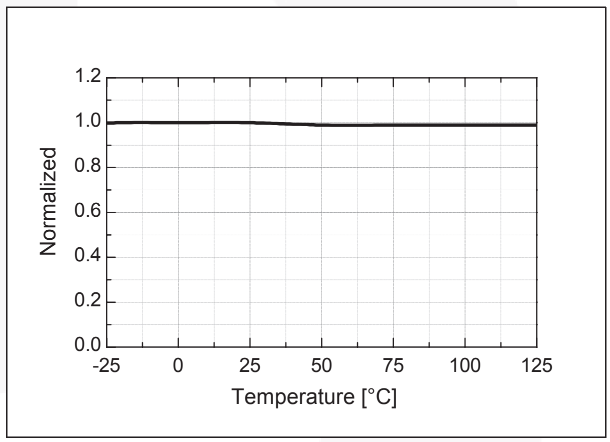

Figure 19. Over-Voltage Protection (V_{OP}) vs. T_A

Functional Description

1. Startup: At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_a) connected to the Vcc pin, as illustrated in Figure 20. When V_{CC} reaches 12V, the FPS begins switching and the internal high-voltage current source is disabled. The FPS continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 8V.

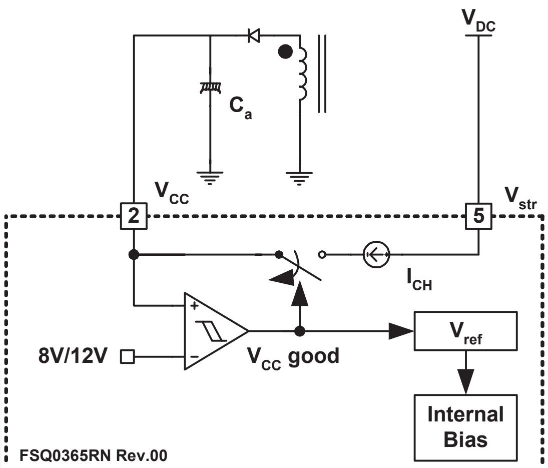

Figure 20. Start-up Circuit

2. Feedback Control: FPS employs current mode control, as shown in Figure 21. An opto-coupler (such as the FOD817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{SENSE} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, thus pulling down the feedback voltage and reducing the duty cycle. This event typically happens when the input voltage is increased or the output load is decreased.

2.1 Pulse-by-Pulse Current Limit: Because current mode control is employed, the peak current through the SenseFET is limited by the inverting input of PWM comparator (V_{FB}*), as shown in Figure 21. Assuming that the 0.9mA current source flows only through the internal resistor (3R + R = 2.8k), the cathode voltage of diode D2 is about 2.5V. Since D1 is blocked when the feedback voltage (V_{FB}) exceeds 2.5V, the maximum voltage of the cathode of D2 is clamped at this voltage, thus clamping V_{FB}*. Therefore, the peak value of the current through the SenseFET is limited.

2.2 Leading Edge Blanking (LEB): At the instant the internal SenseFET is turned on, a high-current spike usually occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{sense} resistor would lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

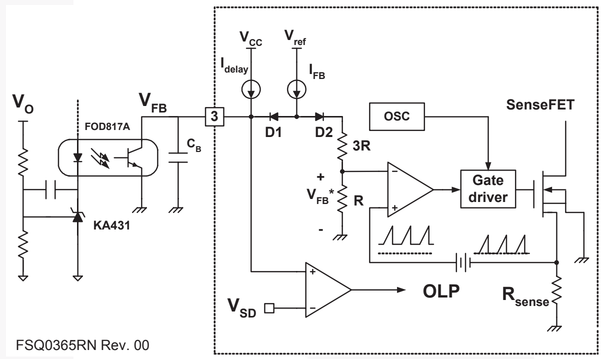

Figure 21. Pulse-Width-Modulation (PWM) Circuit

3. Synchronization: The FSQ-series employs a valley switching technique to minimize the switching noise and loss. The basic waveforms of the valley switching converter are shown in Figure 22. To minimize the MOSFET's switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value, as shown in Figure 22. The minimum drain voltage is indirectly detected by monitoring the V_{CC} winding voltage, as shown in Figure 22.

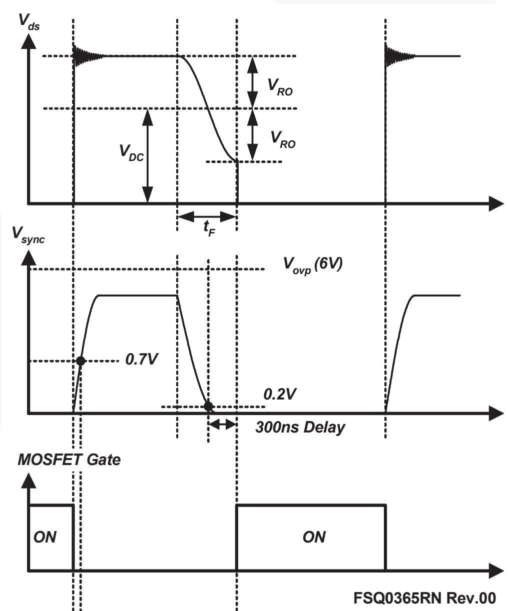

Figure 22. Valley Resonant Switching Waveforms

4. Protection Circuits: The FSQ-series has several self-protective functions, such as Overload Protection (OLP), Abnormal Over-Current protection (AOCP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart mode. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls down to the Under-Voltage Lockout (UVLO) stop voltage of 8V, the protection is reset and start-up circuit charges V_{CC} capacitor. When the V_{CC} reaches the start voltage of 12V, the FSQ-series resumes normal operation. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, the reliability is improved without increasing cost.

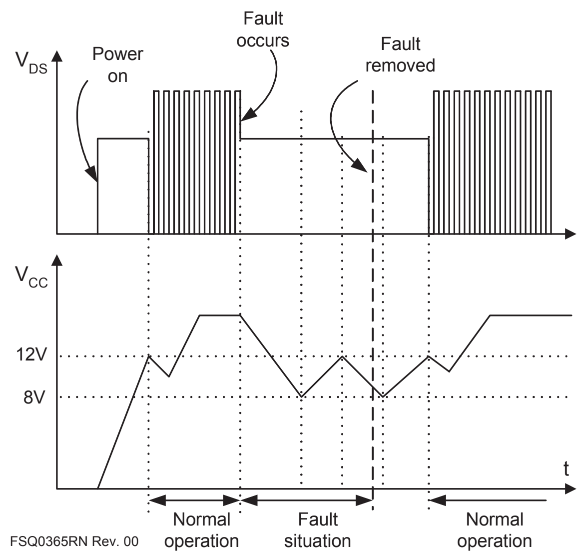

Figure 23. Auto Restart Protection Waveforms

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in the normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the Sense FET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_O) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.8V, D1 is blocked and the 5µA current source starts to charge CB slowly up to V_{CC}. In this condition, V_{FB} continues increasing until it reaches 6V, when the switching operation is terminated, as shown in Figure 24. The delay time for shutdown is the time required to charge CB from 2.8V to 6V with 5µA. A 20 ~ 50ms delay time is typical for most applications.

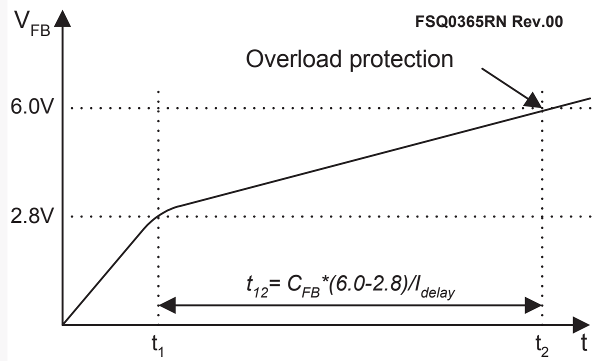

Figure 24. Overload Protection

4.2 Abnormal Over-Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high-di/dt can flow through the SenseFET during the LEB time. Even though the FSQ-series has OLP (Overload Protection), it is not enough to protect the FSQ-series in that abnormal case, since severe current stress is imposed on the SenseFET until OLP triggers. The FSQ-series has an internal AOCP (Abnormal Over-Current Protection) circuit as shown in Figure 25. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the latch, resulting in the shutdown of the SMPS.

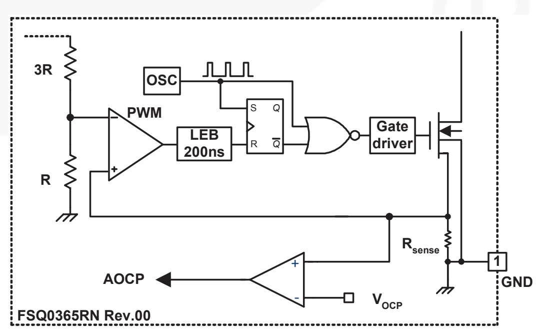

Figure 25. Abnormal Over-Current Protection

4.3 Over-Voltage Protection (OVP): If the secondary side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then, V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection triggers. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection triggers, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the peak voltage of the sync signal is proportional to the output voltage and the FSQ-series uses a sync signal instead of directly monitoring the output voltage. If the sync signal exceeds 6V, an OVP is triggered, shutting down the SMPS. To avoid undesired triggering of OVP during normal operation, the peak voltage of the sync signal should be designed below 6V.

4.4 Thermal Shutdown (TSD): The SenseFET and the control IC are built in one package. This makes it easy for the control IC to detect the abnormal over temperature of the SenseFET. If the temperature exceeds ~150°C, the thermal shutdown triggers.

5. Soft-Start: The FPS has an internal soft-start circuit that increases PWM comparator inverting input voltage with the SenseFET current slowly after it starts up. The typical soft-start time is 15ms, The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. This mode helps prevent transformer saturation and reduces stress on the secondary diode during startup.

6. Burst Operation: To minimize power dissipation in standby mode, the FPS enters burst-mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 26, the device automatically enters burst-mode when the feedback voltage drops below V_{BURL} (350mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (550mV), switching resumes. The feedback voltage then falls and the process repeats. Burst-mode operation alternately enables and disables switching of the power SenseFET, thereby reducing switching loss in standby mode.

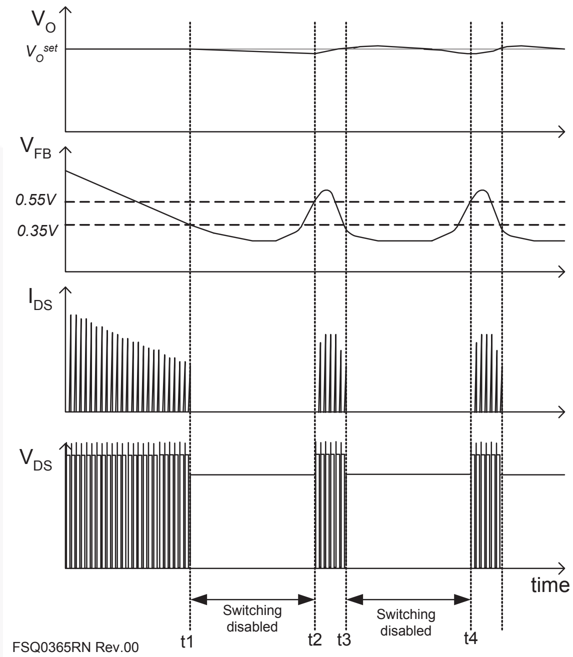

Figure 26. Waveforms of Burst Operation

7. Switching Frequency Limit: To minimize switching loss and EMI (Electromagnetic Interference), the MOSFET turns on when the drain voltage reaches its minimum value in valley switching operation. However, this causes switching frequency to increases at light load conditions. As the load decreases, the peak drain current diminishes and the switching frequency increases. This results in severe switching losses at light-load condition, as well as intermittent switching and audible noise. Because of these problems, the valley switching converter topology has limitations in a wide range of applications.

To overcome this problem, FSQ-series employs a frequency-limit function, as shown in Figures 27 and 28. Once the SenseFET is turned on, the next turn-on is prohibited during the blanking time (t_B). After the blanking time, the controller finds the valley within the detection time window (t_W) and turns on the MOSFET, as shown in Figures 27 and 28 (Cases A, B, and C). If no valley is found during t_W, the internal SenseFET is forced to turn on at the end of t_W (Case D). Therefore, our devices have a minimum switching frequency of 55kHz and a maximum switching frequency of 67kHz, as shown in Figure 28.

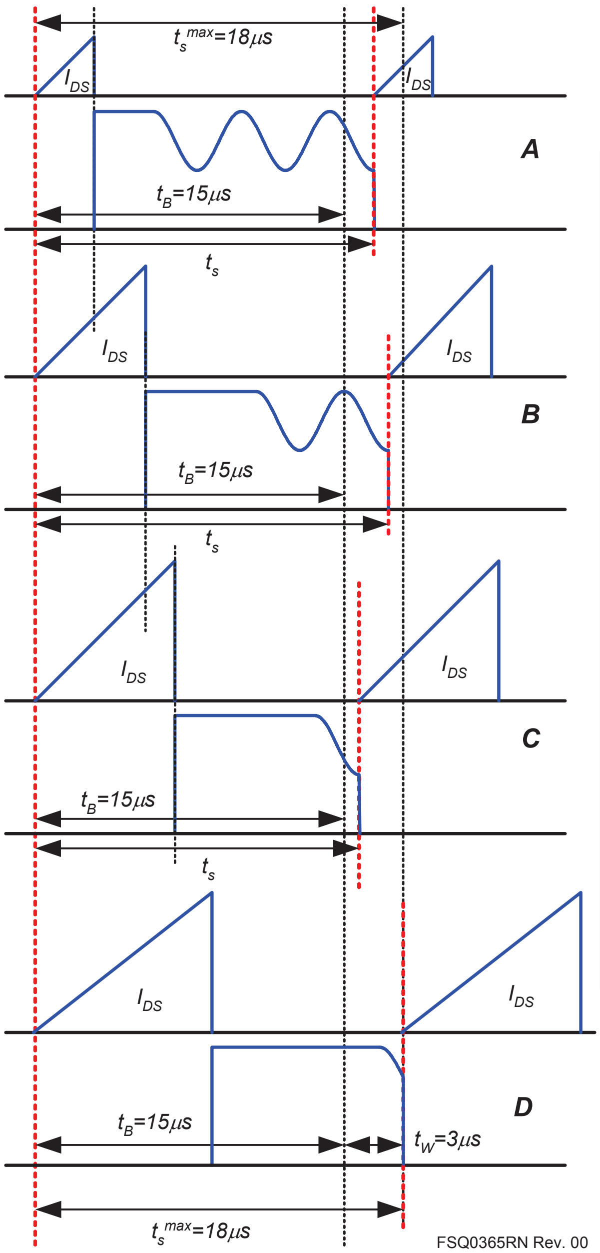

Figure 27. Valley Switching with Limited Frequency

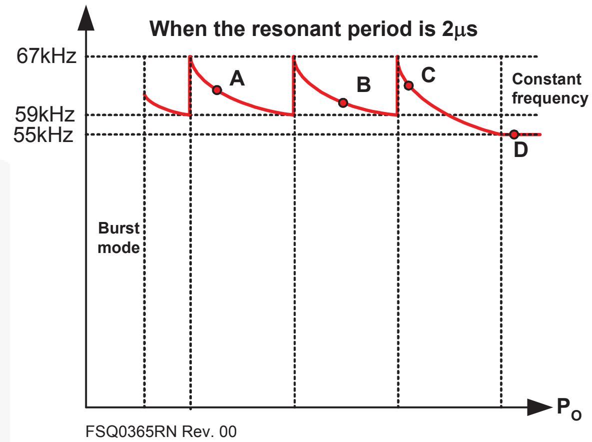

Figure 28. Switching Frequency Range

Typical Application Circuit of FSQ0365RN

Application	FPS Device	Input Voltage Range	Rated Output Power	Output Voltage (Max. Current)
DVD Player Power Supply	FSQ0365RN	85-265V_{AC}	19W	5.1V (1.0A) 3.4V (1.0A) 12V (0.4A) 16V (0.3A)

Features

- High efficiency (>77% at universal input)
- Low standby mode power consumption (<1W at 230V_{AC} input and 0.5W load)
- Reduce EMI noise through Valley Switching operation
- Enhanced system reliability through various protection functions
- Internal soft-start (15ms)

Key Design Notes

- The delay time for overload protection is designed to be about 30ms with C107 of 47nF. If faster/slower triggering of OLP is required, C107 can be changed to a smaller/larger value (eg. 100nF for 60ms).
- The input voltage of V_{sync} must be higher than -0.3V. By proper voltage sharing by R106 & R107 resistors, the input voltage can be adjusted.
- The SMD-type 100nF capacitor must be placed as close as possible to V_{CC} pin to avoid malfunction by abrupt pulsating noises and to improved surge immunity.

1. Schematic

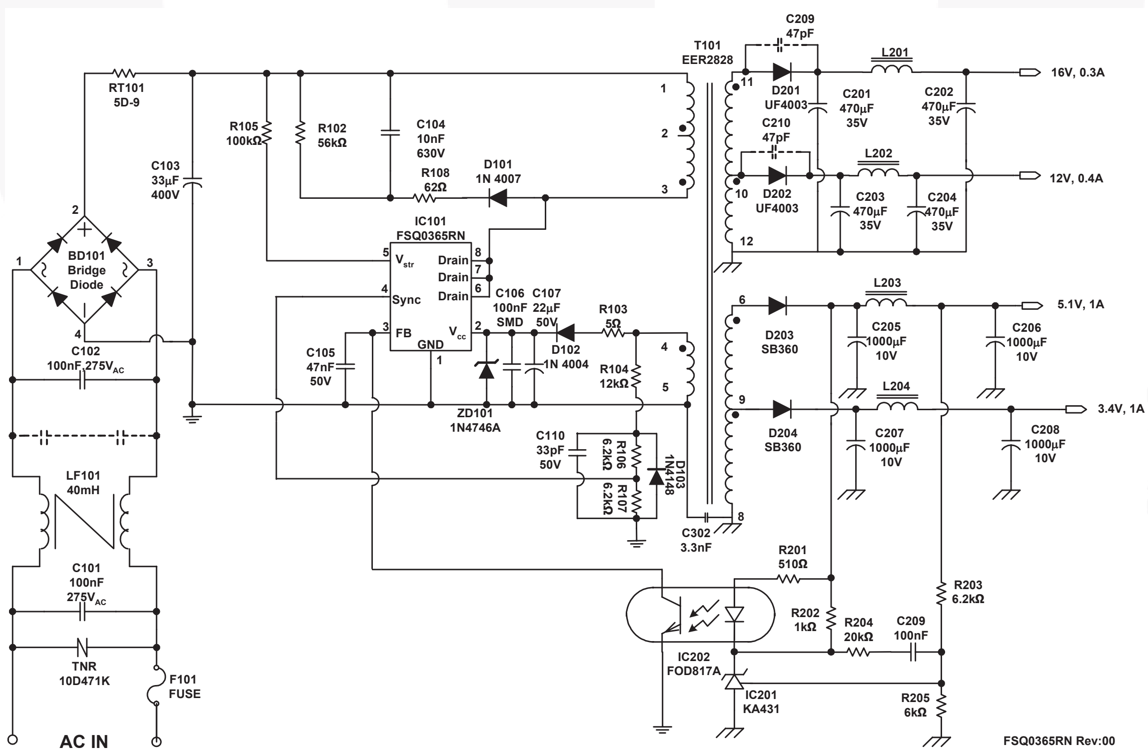

Figure 29. Demo Circuit of FSQ0365RN

2. Transformer

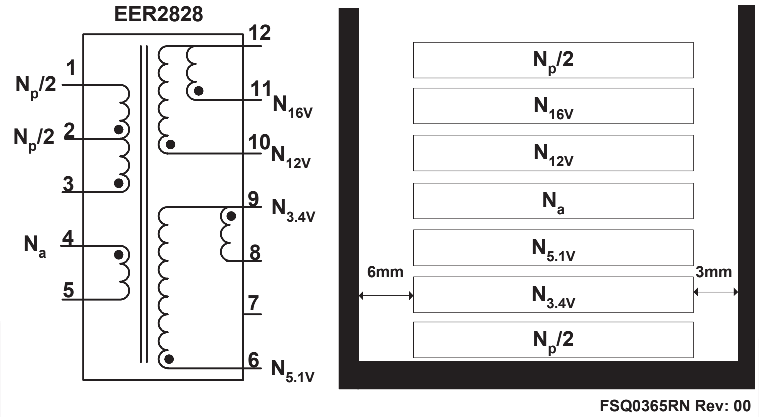

Figure 30. Transformer Schematic Diagram of FSQ0365RN

3. Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
$N_p/2$	3 → 2	$0.25^{\phi} \times 1$	50	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2 Layers				
$N_{3.4V}$	9 → 8	$0.33^{\phi} \times 2$	4	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2 Layers				
N_{5V}	6 → 9	$0.33^{\phi} \times 1$	2	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2 Layers				
N_a	4 → 5	$0.25^{\phi} \times 1$	16	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2 Layers				
N_{12V}	10 → 12	$0.33^{\phi} \times 3$	14	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 3 Layers				
N_{16V}	11 → 12	$0.33^{\phi} \times 3$	18	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2 Layers				
$N_p/2$	2 → 1	$0.25^{\phi} \times 1$	50	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2 Layers				

4. Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 3	1.4mH ± 10%	100kHz, 1V
Leakage	1 - 3	25μH Max.	Short all other pins

5. Core & Bobbin

- Core: EER2828 (Ae=86.66mm^2)
- Bobbin: EER2828

6. Demo Board Part List

Part	Value	Note	Part	Value	Note
Resistor			**Inductor**		
R102	56kΩ	1W	L201	10µH	
R103	5Ω	1/2W	L202	10µH	
R104	12kΩ	1/4W	L203	4.9µH	
R105	100kΩ	1/4W	L204	4.9µH	
R106	6.2kΩ	1/4W	**Diode**		
R107	6.2kΩ	1/4W	D101	IN4007	
R108	62Ω	1W	D102	IN4004	
R201	510Ω	1/4W	ZD101	1N4746A	
R202	1kΩ	1/4W	D103	1N4148	
R203	6.2kΩ	1/4W	D201	UF4003	
R204	20kΩ	1/4W	D202	UF4003	
R205	6kΩ	1/4W	D203	SB360	
Capacitor			D204	SB360	
C101	100nF/275V_{AC}	Box Capacitor			
C102	100nF/275V_{AC}	Box Capacitor	**IC**		
C103	33µF/400V	Electrolytic Capacitor	IC101	FSQ0365RN	FPS™
C104	10nF/630V	Film Capacitor	IC201	KA431 (TL431)	Voltage reference
C105	47nF/50V	Mono Capacitor	IC202	FOD817A	Opto-coupler
C106	100nF/50V	SMD (1206)	**Fuse**		
C107	22µF/50V	Electrolytic Capacitor	Fuse	2A/250V	
C110	33pF/50V	Ceramic Capacitor	**NTC**		
C201	470µF/35V	Electrolytic Capacitor	RT101	5D-9	
C202	470µF/35V	Electrolytic Capacitor	**Bridge Diode**		
C203	470µF/35V	Electrolytic Capacitor	BD101	2KBP06M2N257	Bridge Diode
C204	470µF/35V	Electrolytic Capacitor	**Line Filter**		
C205	1000µF/10V	Electrolytic Capacitor	LF101	40mH	
C206	1000µF/10V	Electrolytic Capacitor	**Transformer**		
C207	1000µF/10V	Electrolytic Capacitor	T101		
C208	1000µF/10V	Electrolytic Capacitor	**Varistor**		
C209	100nF /50V	Ceramic Capacitor	TNR	10D471K	

Typical Application Circuit of FSQ311

Application	FPS Device	Input Voltage Range	Rated Output Power	Output Voltage (Max. Current)
DVD Player Power Supply	FSQ311	85-265V_{AC}	8W	5.1V (0.9A) 3.3V (0.9A) 12V (0.03A) 16V (0.03A)

Features

- High efficiency (>70% at universal input)
- Low standby mode power consumption (<1W at 230V_{AC} input and 0.5W load)
- Reduce EMI noise through Valley Switching operation
- Enhanced system reliability through various protection functions
- Internal soft-start (15ms)

Key Design Notes

- The delay time for overload protection is designed to be about 30ms with C107 of 47nF. If faster/slower triggering of OLP is required, C107 can be changed to a smaller/larger value (eg. 100nF for 60ms).
- The input voltage of V_{sync} must be higher than -0.3V. By proper voltage sharing by R106 & R107 resistors, the input voltage can be adjusted.
- The SMD-type 100nF capacitor must be placed as close as possible to V_{CC} pin to avoid malfunction by abrupt pulsating noises and to improved surge immunity.

1. Schematic

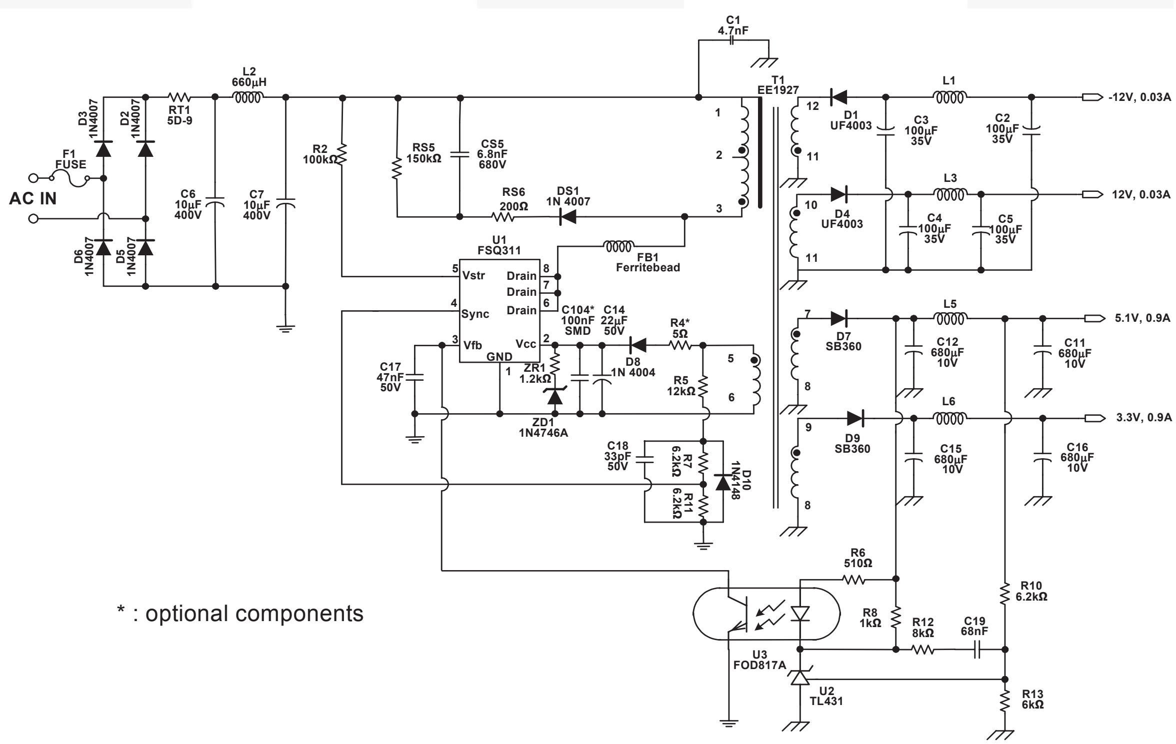

Figure 31. Demo Circuit of FSQ311

2. Transformer

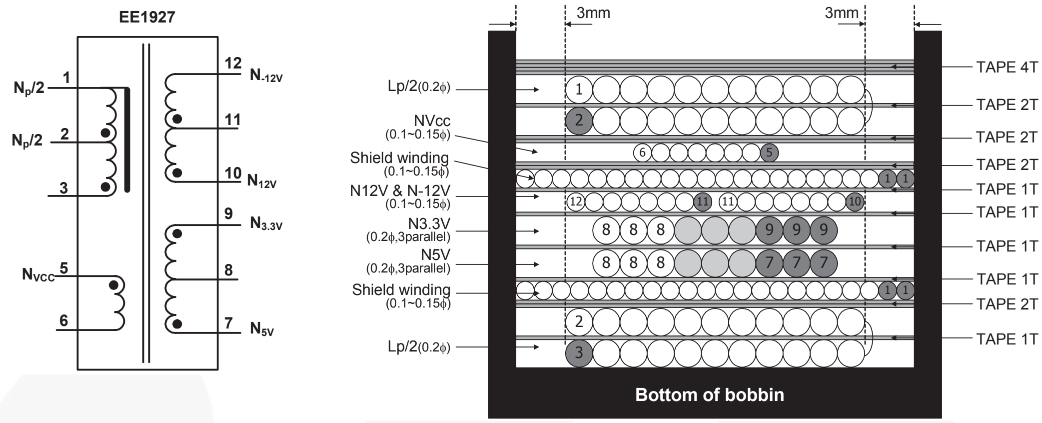

Figure 32. Transformer Schematic Diagram of FSQ311

3. Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
$N_p/2$	3 → 2	$0.2^{\phi} \times 1$	111	Solenoid Winding, 2 Layers
Insulation: Polyester Tape t = 0.025mm, 2 Layers				
Shield	1 → open	$0.1^{\phi} \times 2$		Shield winding
Insulation: Polyester Tape t = 0.025mm, 1 Layer				
N_{5V}	7 → 8	$0.2^{\phi} \times 3$	15	Center Solenoid Winding
Insulation: Polyester Tape t = 0.025mm, 1 Layer				
$N_{3.3V}$	9 → 8	$0.2^{\phi} \times 3$	10	Center Solenoid Winding
Insulation: Polyester Tape t = 0.025mm, 1 Layer				
N_{12V}	10 → 11	$0.1^{\phi} \times 1$	30	Solenoid Winding
N_{-12V}	11 → 12	$0.1^{\phi} \times 3$	33	Solenoid Winding
Insulation: Polyester Tape t = 0.025mm, 1 Layer				
Shield	1 → open	$0.1^{\phi} \times 2$		Shield winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				
N_{VCCV}	5 → 6	$0.1^{\phi} \times 1$	36	Center Solenoid Winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				
$N_p/2$	2 → 1	$0.2^{\phi} \times 1$	111	Solenoid Winding, 2 Layers
Insulation: Polyester Tape t = 0.025mm, 4 Layers				

4. Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 3	2.1mH ± 10%	66kHz, 1V
Leakage	1 - 3	100μH Max.	Short all other pins

5. Core & Bobbin

- Core: EE1927 (Ae=23.4mm^2)
- Bobbin: EE1927

6. Demo Board Part List

Part	Value	Note	Part	Value	Note
Resistor			**Inductor**		
R2	100kΩ	1/4W	L2	660µH	
ZR1	1.2kΩ	1/4W	L1	4.7µH	
R4	5Ω	1/2W	L3	4.7µH	
R5	12kΩ	1/4W	L5	4.7µH	
R7	6.2kΩ	1/4W	L6	4.7µH	
R11	6.2kΩ	1/4W	**Diode**		
RS5	150kΩ	2W	D2,3,4,5	IN4007	
RS6	200Ω	1W	D8	IN4004	
R6	510Ω	1/4W	D10	1N4148	
R8	1kΩ	1/4W	ZD1	1N4746A	
R12	8kΩ	1/4W	DS1	1N4007	
R10	6.2kΩ	1/4W, 1%	D1	UF4003	
R13	6kΩ	1/4W, 1%	D4	UF4003	
Capacitor			D7	SB360	
C6	10µF/400V	Electrolytic	D9	SB360	
C7	10µF/400V	Electrolytic	**IC**		
C17	47nF/50V	Ceramic	U1	FSQ311	FPS™
C104	100nF/50V	SMD(1206)	U2	KA431 (TL431)	Voltage reference
C14	22µF/50V	Electrolytic	U3	FOD817A	Opto-coupler
C18	33pF/50V	Ceramic	**Fuse**		
CS5	6.8nF/680V	Film	Fuse	2A/250V	
C2	100µF/35V	Electrolytic	**NTC**		
C3	100µF/35V	Electrolytic	RT1	5D-9	
C4	100µF/35V	Electrolytic	**Transformer**		
C5	100µF/35V	Electrolytic	T1	EE1927	Bridge Diode
C11	680µF/10V	Electrolytic	**Ferrite bead**		
C12	680µF/10V	Electrolytic	FB1		
C15	680µF/10V	Electrolytic			
C16	680µF/10V	Electrolytic			
C19	68nµF/50V	Ceramic			
C1	4.7nF/375V_{AC}	Ceramic			

Package Dimensions

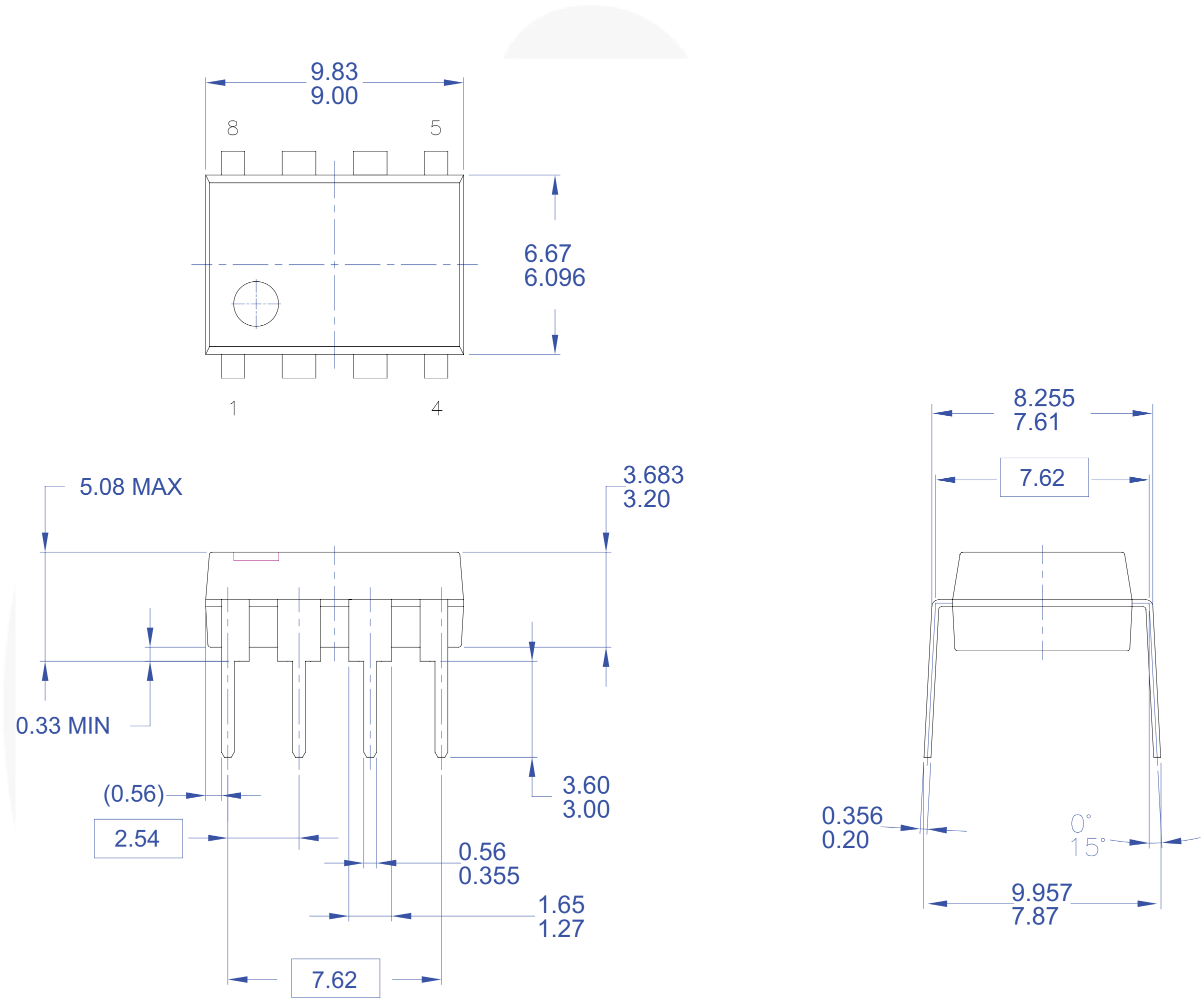

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Figure 33. 8-Lead, Dual In-Line Package(DIP)

Package Dimensions (Continued)

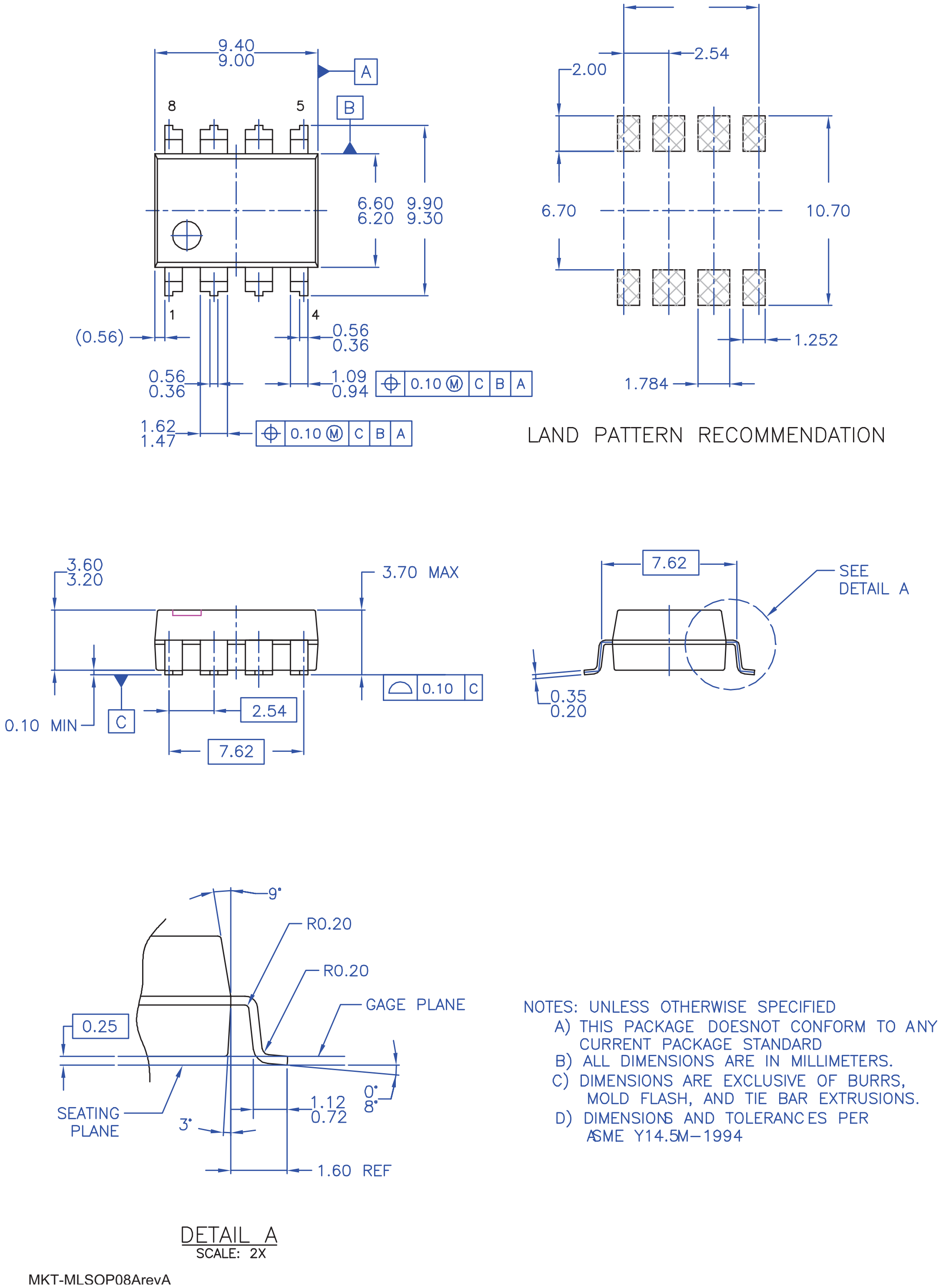

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Figure 34. 8-Lead, LSOP Package

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