LM5017

100V, 600mA Constant On-Time Synchronous Buck Regulator

General Description

The LM5017 is a 100V, 600mA synchronous step-down regulator with integrated high side and low side MOSFETs. The constant-on-time (COT) control scheme employed in the LM5017 requires no loop compensation, provides excellent transient response, and enables very low step-down ratios. The on-time varies inversely with the input voltage resulting in nearly constant frequency over the input voltage range. A high voltage startup regulator provides bias power for internal operation of the IC and for integrated gate drivers.

A peak current limit circuit protects against overload conditions. The undervoltage lockout (UVLO) circuit allows the input undervoltage threshold and hysteresis to be independently programmed. Other protection features include thermal shutdown and bias supply undervoltage lockout (V_{CC} UVLO).

The LM5017 is available in LLP-8 and PSOP-8 plastic packages.

Features

- Wide 9V to 100V Input Range
- Integrated 100V, High and Low Side Switches
- No Schottky Required
- Constant On-time Control
- No Loop Compensation Required
- Ultra-Fast Transient Response
- Nearly Constant Operating Frequency
- Intelligent Peak Current Limit
- Adjustable Output Voltage from 1.225V
- Precision 2% Feedback Reference
- Frequency Adjustable to 1MHz
- Adjustable Undervoltage Lockout (UVLO)
- Remote Shutdown
- Thermal Shutdown

Packages

- LLP-8
- PSOP-8

Applications

- Smart Power Meters
- Telecommunication Systems
- Automotive Electronics
- Isolated Bias Supply

Typical Application

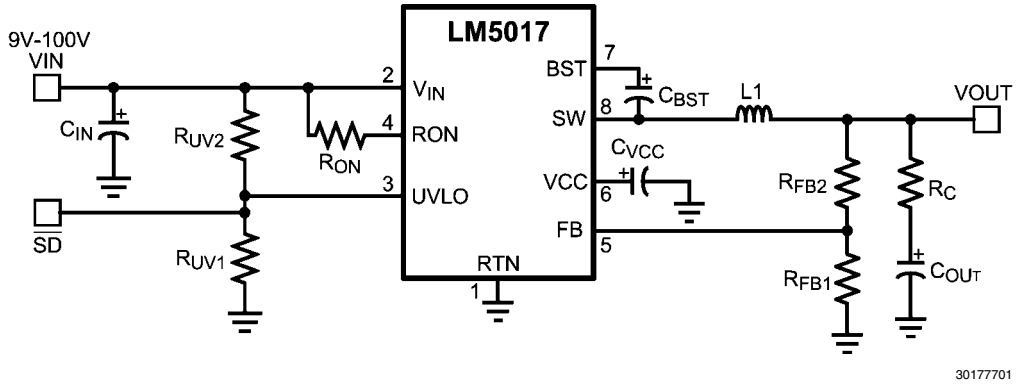
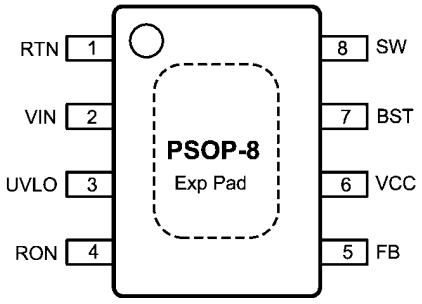
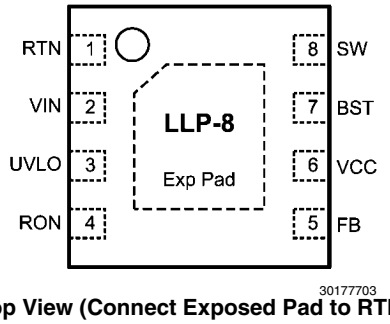


FIGURE 1.

Connection Diagram



Top View (Connect Exposed Pad to RTN)



Top View (Connect Exposed Pad to RTN)

Ordering Information

Order Number	Package Type	Package Drawing	Supplied As
LM5017MR	PSOP-8	MRA08A	95 Units in a Rail
LM5017MRE	PSOP-8	MRA08A	250 Units on Tape and Reel
LM5017MRX	PSOP-8	MRA08A	1000 Units on Tape and Reel
LM5017SD	LLP-8	SDC08B	1000 Units on Tape and Reel
LM5017SDE	LLP-8	SDC08B	250 Units on Tape and Reel
LM5017SDX	LLP-8	SDC08B	4500 Units on Tape and Reel

Pin Descriptions

Pin	Name	Description	Application Information
1	RTN	Ground	Ground connection of the integrated circuit.
2	V_{IN}	Input Voltage	Operating input range is 9V to 100V.
3	UVLO	Input Pin of Undervoltage Comparator	Resistor divider from V_{IN} to UVLO to GND programs the undervoltage detection threshold. An internal current source is enabled when UVLO is above 1.225V to provide hysteresis. When UVLO pin is pulled below 0.66V externally, the parts goes in shutdown mode.
4	R_{ON}	On-Time Control	A resistor between this pin and V_{IN} sets the switch on-time as a function of V_{IN}. Minimum recommended on-time is 100ns at max input voltage.
5	FB	Feedback	This pin is connected to the inverting input of the internal regulation comparator. The regulation level is 1.225V.
6	V_{CC}	Output from the Internal High Voltage Series Pass Regulator. Regulated at 7.6V	The internal V_{CC} regulator provides bias supply for the gate drivers and other internal circuitry. A 1.0µF decoupling capacitor is recommended.
7	BST	Bootstrap Capacitor	An external capacitor is required between the BST and SW pins (0.01µF ceramic). The BST pin capacitor is charged by the V_{CC} regulator through an internal diode when the SW pin is low.
8	SW	Switching Node	Power switching node. Connect to the output inductor and bootstrap capacitor.
	EP	Exposed Pad	Exposed pad must be connected to RTN pin. Connect to system ground plane on application board for reduced thermal resistance.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

V_{IN}, UVLO to RTN	-0.3V to 100V
SW to RTN	-1.5V to V_{IN} +0.3V
BST to V_{CC}	100V
BST to SW	13V
R_{ON} to RTN	-0.3V to 100V
V_{CC} to RTN	-0.3V to 13V
FB to RTN	-0.3V to 5V
ESD Rating (Human Body Model(Note 5)	2kV
Lead Temperature (Note 2)	200°C
Storage Temperature Range	-55°C to +150°C

Operating Ratings (Note 1)

V_{IN} Voltage	9V to 100V
Operating Junction Temperature	−40°C to +125°C

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** type apply over full Operating Junction Temperature range. V_{IN} = 48V, unless otherwise stated. See (Note 3).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC} Supply						
V_{CC} Reg	V_{CC} Regulator Output	V_{IN} = 48V, I_{CC} = 20mA	**6.25**	7.6	**8.55**	V
	V_{CC} Current Limit	V_{IN} = 48V(Note 4)	**26**			mA
	V_{CC} Undervoltage Lockout Voltage (V_{CC} increasing)		**4.15**	4.5	**4.9**	V
	V_{CC} Undervoltage Hysteresis			300		mV
	V_{CC} Drop Out Voltage	V_{IN} = 9V, I_{CC} = 20mA		2.3		V
	I_{IN} Operating Current	Non-Switching, FB = 3V		1.75		mA
	I_{IN} Shutdown Current	UVLO = 0V		50	**225**	µA
Switch Characteristics						
	Buck Switch $R_{DS(ON)}$	I_{TEST} = 200mA, BST-SW = 7V		0.8	**1.8**	Ω
	Synchronous $R_{DS(ON)}$	I_{TEST} = 200mA		0.45	**1**	Ω
	Gate Drive UVLO	$V_{BST} - V_{SW}$ Rising	**2.4**	3	**3.6**	V
	Gate Drive UVLO Hysteresis			260		mV
Current Limit						
	Current Limit Threshold		**0.7**	1.02	**1.3**	A
	Current Limit Response Time	Time to Switch Off		150		ns
	OFF-Time Generator (Test 1)	FB = 0.1V, V_{IN} = 48V		12		µs
	OFF-Time Generator (Test 2)	FB = 1.0V, V_{IN} = 48V		2.5		µs
On-Time Generator						
	T_{ON} Test 1	V_{IN} = 32V, R_{ON} = 100k	**270**	350	**460**	ns
	T_{ON} Test 2	V_{IN} = 48V, R_{ON} = 100k	**188**	250	**336**	ns
	T_{ON} Test 3	V_{IN} = 75V, R_{ON} = 250k	**250**	370	**500**	ns
	T_{ON} Test 4	V_{IN} = 10V, R_{ON} = 250k	**1880**	3200	**4425**	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Minimum Off-Time						
	Minimum Off-Timer	FB = 0V		144		ns
Regulation and Overvoltage Comparators						
	FB Regulation Level	Internal Reference Trip Point for Switch ON	**1.2**	1.225	**1.25**	V
	FB Overvoltage Threshold	Trip Point for Switch OFF		1.62		V
	FB Bias Current			60		nA
Undervoltage Sensing Function						
	UV Threshold	UV Rising	**1.19**	1.225	**1.26**	V
	UV Hysteresis Input Current	UV = 2.5V	**-10**	-20	**-29**	µA
	Remote Shutdown Threshold	Voltage at UVLO Falling	**0.32**	0.66		V
	Remote Shutdown Hysteresis			110		mV
Thermal Shutdown						
Tsd	Thermal Shutdown Temperature			165		°C
	Thermal Shutdown Hysteresis			20		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient	PSOP-8		40		°C/W
		LLP-8		40		°C/W

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics. The RTN pin is the GND reference electrically connected to the substrate.

Note 2: For detailed information on soldering plastic PSOP package, refer to the Packaging Data Book available from National Semiconductor Corporation. Max solder time not to exceed 4 seconds.

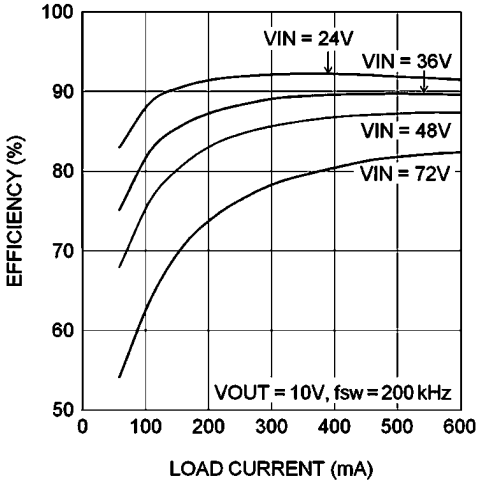
Note 3: All limits are guaranteed by design. All electrical characteristics having room temperature limits are tested during production at T_A = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 4: V_{CC} provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

Note 5: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Typical Performance Characteristics

Efficiency at 200kHz, 10V



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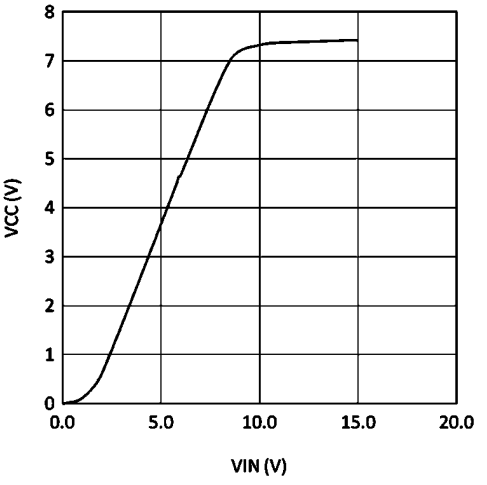
V_{CC} vs V_{IN}



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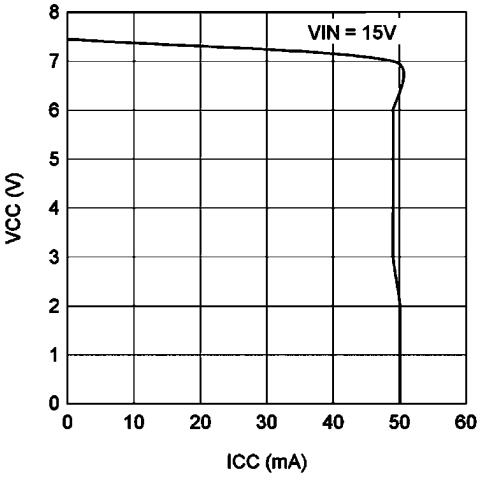
V_{CC} vs I_{CC}



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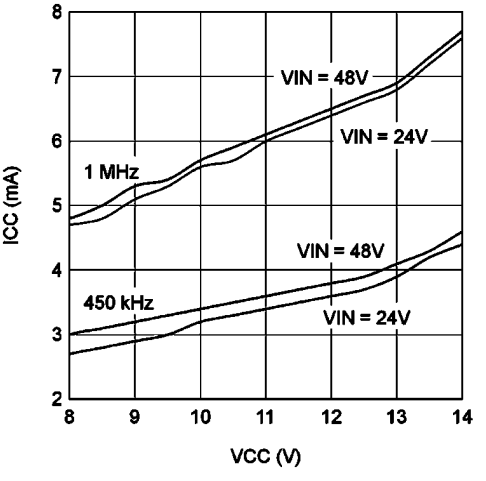
I_{CC} vs External V_{CC}



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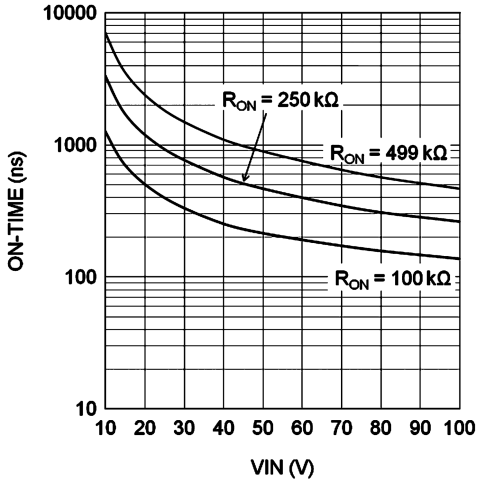
T_{ON} vs V_{IN} and R_{ON}



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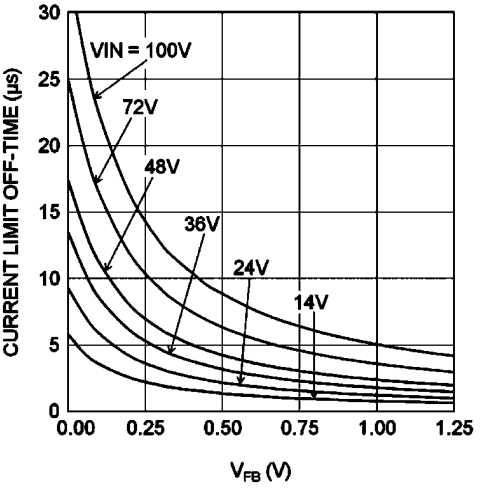
T_{OFF} (I_{LIM}) vs V_{FB} and V_{IN}



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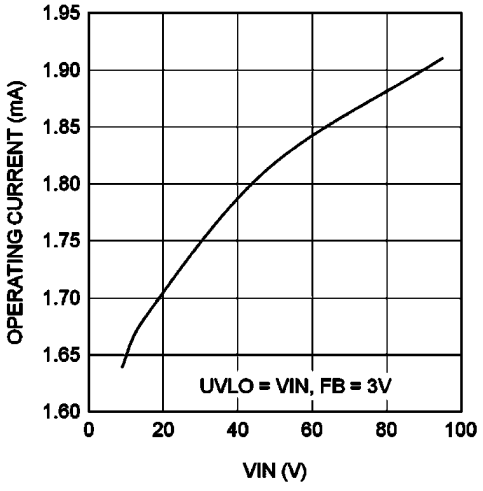
I_{IN} vs V_{IN} (Operating, Non Switching)



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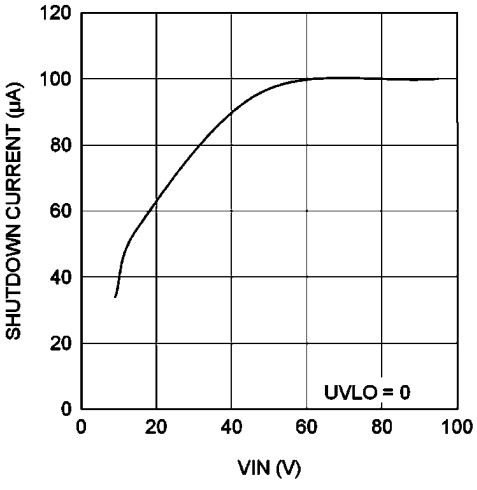
I_{IN} vs V_{IN} (Shutdown)



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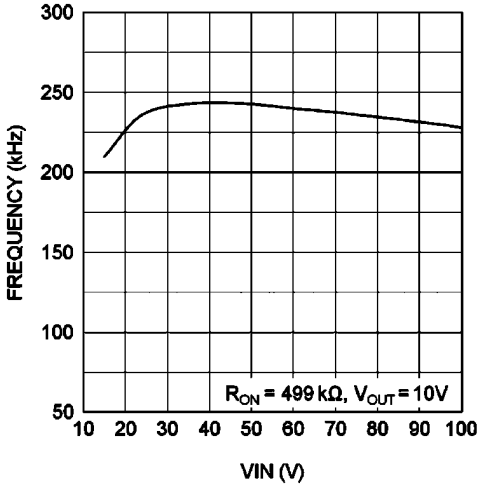
Switching Frequency vs V_{IN}



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Block Diagram

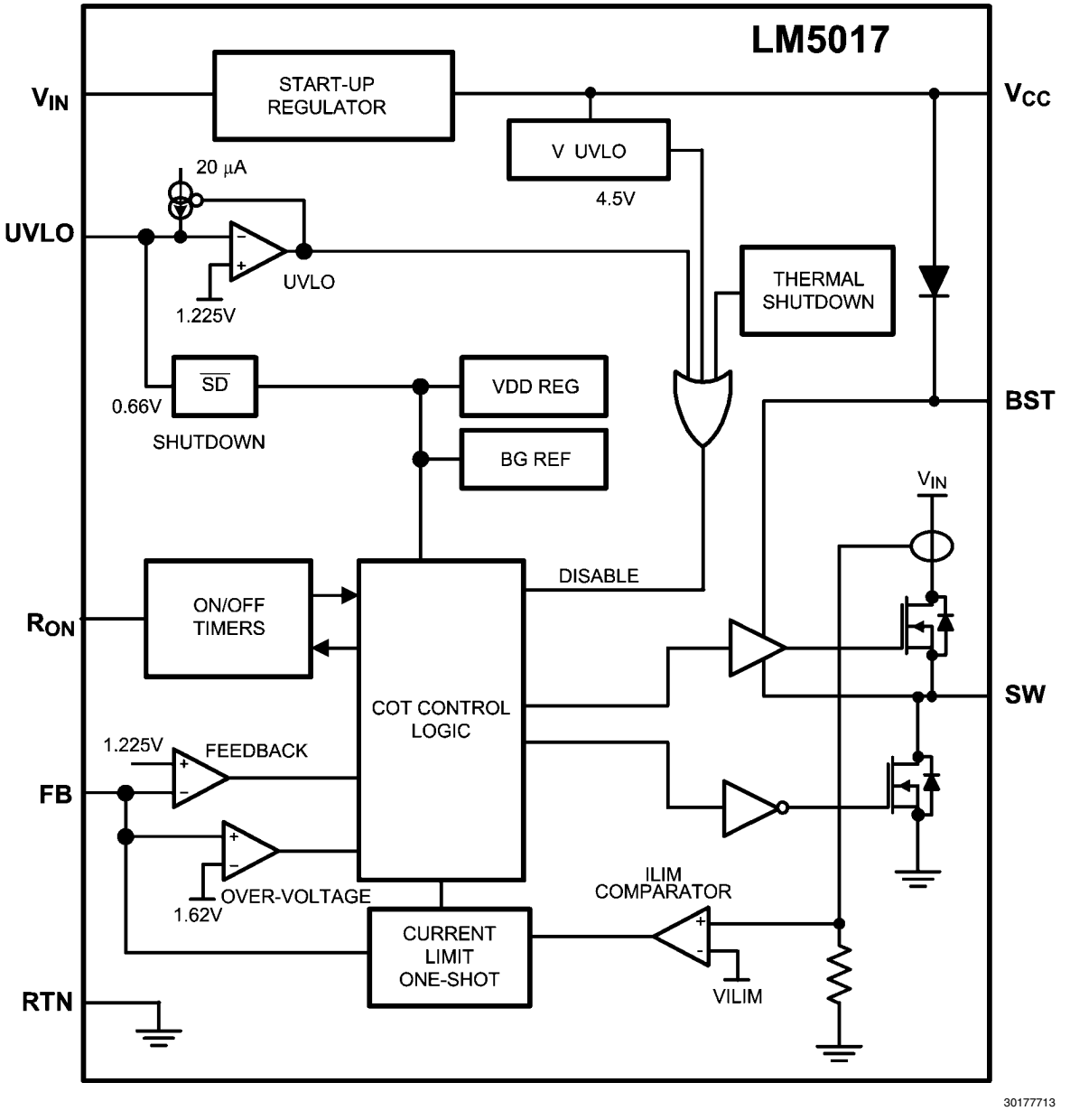


FIGURE 2. Functional Block Diagram

Functional Description

The LM5017 step-down switching regulator features all the functions needed to implement a low cost, efficient, buck converter capable of supplying up to 0.6A to the load. This high voltage regulator contains 100V, N-channel buck and synchronous switches, is easy to implement, and is provided in thermally enhanced PSOP-8 and LLP-8 packages. The regulator operation is based on a constant on-time control scheme using an on-time inversely proportional to V_{IN}. This control scheme does not require loop compensation. The current limit is implemented with a forced off-time inversely proportional to V_{OUT}. This scheme ensures short circuit protection while providing minimum foldback. The simplified block diagram of the LM5017 is shown in *Figure 2*, Functional Block Diagram.

The LM5017 can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well suited for 48V telecom and 42V automotive power bus ranges. Protection features include: thermal shutdown, Undervoltage Lockout (UVLO), minimum forced off-time, and an intelligent current limit.

Control Overview

The LM5017 buck regulator employs a control principle based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (1.225V). If the FB voltage is below the reference the internal buck switch is turned on for the one-shot timer period, which is a function of the input voltage and the programming resistor (R_{ON}). Following the on-time the switch remains off until the FB voltage falls below the reference, but never before the minimum off-time forced by the minimum off-time one-shot timer. When the FB pin voltage falls below the reference and the minimum off-time one-shot period expires, the buck switch is turned on for another on-time one-shot period. This will continue until regulation is achieved and the FB voltage is approximately equal to 1.225V (typ).

In a synchronous buck converter, the low side (sync) FET is 'on' when the high side (buck) FET is 'off'. The inductor current ramps up when the high side switch is 'on' and ramps down when the high side switch is 'off'. There is no diode emulation feature in this IC, and therefore, the inductor current may ramp in the negative direction at light load. This causes the converter to operate in continuous conduction mode (CCM) regardless of the output loading. The operating frequency remains relatively constant with load and line variations. The operating frequency can be calculated as follows:

$$f_{sw} = \frac{V_{OUT}}{10^{-10} \times R_{ON}}$$

The output voltage (V_{OUT}) is set by two external resistors (R_{FB1}, R_{FB2}). The regulated output voltage is calculated as follows:

$$V_{OUT} = 1.225V \times \frac{R_{FB2} + R_{FB1}}{R_{FB1}}$$

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT} - 1.225V}{1.225V}$$

This regulator regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor (C_{OUT}). A minimum of 25mV of ripple voltage at the feedback pin (FB) is required for the LM5017. In cases where the capacitor ESR is too small, additional series resistance may be required (R_C in *Figure 3* Low Ripple Output Configuration).

For applications where lower output voltage ripple is required the output can be taken directly from a low ESR output capacitor, as shown in *Figure 3* Low Ripple Output Configuration. However, R_C slightly degrades the load regulation.

V_{CC} Regulator

The LM5017 contains an internal high voltage linear regulator with a nominal output of 7.6V. The input pin (V_{IN}) can be connected directly to the line voltages up to 100V. The V_{CC} regulator is internally current limited to 30mA. The regulator sources current into the external capacitor at V_{CC}. This regulator supplies current to internal circuit blocks including the synchronous MOSFET driver and the logic circuits. When the voltage on the V_{CC} pin reaches the undervoltage lockout (V_{CC} UVLO) threshold of 4.5V, the IC is enabled.

The V_{CC} regulator contains an internal diode connection to the BST pin to replenish the charge in the gate drive boot capacitor when SW pin is low.

At high input voltages, the power dissipated in the high voltage regulator is significant and can limit the overall achievable output power. As an example, with the input at 48V and switching at high frequency, the V_{CC} regulator may supply up to 7mA of current resulting in 48V x 7mA = 336mW of power dissipation. If the V_{CC} voltage is driven externally by an alternate voltage source, between 8V and 13V, the internal regulator is disabled. This reduces the power dissipation in the IC.

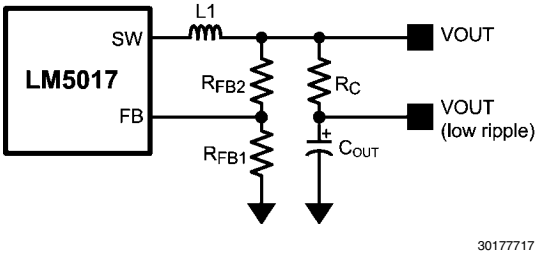


FIGURE 3. Low Ripple Output Configuration

Regulation Comparator

The feedback voltage at FB is compared to an internal 1.225V reference. In normal operation, when the output voltage is in regulation, an on-time period is initiated when the voltage at FB falls below 1.225V. The high side switch will stay on for the on-time, causing the FB voltage to rise above 1.225V. After the on-time period, the high side switch will stay off until the FB voltage again falls below 1.225V. During start-up, the FB voltage will be below 1.225V at the end of each on-time, causing the high side switch to turn on immediately after the minimum forced off-time of 144ns. The high side switch can be turned off before the on-time is over, if the peak current in the inductor reaches the current limit threshold.

Overvoltage Comparator

The feedback voltage at FB is compared to an internal 1.62V reference. If the voltage at FB rises above 1.62V the on-time pulse is immediately terminated. This condition can occur if the input voltage and/or the output load changes suddenly. The high side switch will not turn on again until the voltage at FB falls below 1.225V.

On-Time Generator

The on-time for the LM5017 is determined by the R_{ON} resistor, and is inversely proportional to the input voltage (V_{IN}), resulting in a nearly constant frequency as V_{IN} is varied over its range. The on-time equation for the LM5017 is:

$$T_{ON} = \frac{10^{-10} \times R_{ON}}{V_{IN}}$$

See figure "T_{ON} vs V_{IN} and R_{ON}" in the section "Performance Curves". R_{ON} should be selected for a minimum on-time (at maximum V_{IN}) greater than 100ns, for proper operation. This requirement limits the maximum switching frequency for high V_{IN}.

Current Limit

The LM5017 contains an intelligent current limit off-timer. If the current in the buck switch exceeds 1.02A the present cycle is immediately terminated, and a non-resetable off-timer is initiated. The length of off-time is controlled by the FB voltage and the input voltage V_{IN}. As an example, when FB = 0V and V_{IN} = 48V, the maximum off-time is set to 16µs. This condition occurs when the output is shorted, and during the initial part of start-up. This amount of time ensures safe short circuit operation up to the maximum input voltage of 100V.

In cases of overload where the FB voltage is above zero volts (not a short circuit) the current limit off-time is reduced. Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and start-up time. The off-time is calculated from the following equation:

$$T_{OFF(ILIM)} = \frac{0.07 \times V_{IN}}{V_{FB} + 0.2V}\ \mu s$$

The current limit protection feature is peak limited. The maximum average output will be less than the peak.

N-Channel Buck Switch and Driver

The LM5017 integrates an N-Channel Buck switch and associated floating high voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 0.01uF ceramic capacitor connected between the BST pin and the SW pin provides the voltage to the driver during the on-time. During each off-time, the SW pin is at approximately 0V, and the bootstrap capacitor charges from V_{CC} through the internal diode. The minimum off-timer, set to 144ns , ensures a minimum time each cycle to recharge the bootstrap capacitor.

Synchronous Rectifier

The LM5017 provides an internal synchronous N-Channel MOSFET rectifier. This MOSFET provides a path for the inductor current to flow when the high-side MOSFET is turned off.

The synchronous rectifier has no diode emulation mode, and is designed to keep the regulator in continuous conduction mode even during light loads which would otherwise result in discontinuous operation.

Undervoltage Detector

The LM5017 contains a dual level undervoltage lockout (UVLO) circuit. When the UVLO pin voltage is below 0.66V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.66V but less than 1.225V, the controller is in standby mode. In standby mode the V_{CC} bias regulator is active while the regulator output is disabled. When the V_{CC} pin exceeds the V_{CC} undervoltage threshold and the UVLO pin voltage is greater than 1.225V, normal operation begins. An external set-point voltage divider from V_{IN} to GND can be used to set the minimum operating voltage of the regulator.

UVLO hysteresis is accomplished with an internal 20µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to quickly raise the voltage at the UVLO pin. The hysteresis is equal to the value of this current times the resistance R_{UV2}.

UVLO	V_{CC}	Mode	Description
<0.66V		Shutdown	V_{CC} regulator disabled. Switcher disabled.
0.66V – 1.225V		Standby	V_{CC} regulator enabled Switcher disabled.
>1.225V	V_{CC} <4.5V	Standby	V_{CC} regulator enabled. Switcher disabled.
	V_{CC} >4.5V	Operating	V_{CC} enabled. Switcher enabled.

If the UVLO pin is wired directly to the V_{IN} pin, the regulator will begin operation once the V_{CC} undervoltage is satisfied.

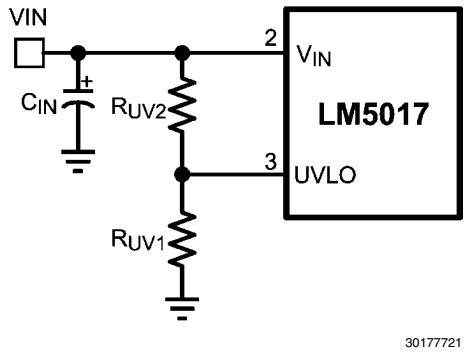


FIGURE 4. UVLO Resistor Setting

Thermal Protection

The LM5017 should be operated so the junction temperature does not exceed 150°C during normal operation. An internal Thermal Shutdown circuit is provided to protect the LM5017 in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low power reset state, disabling the buck switch and the V_{CC} regulator. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 145°C (typical hysteresis = 20°C), the V_{CC} regulator is enabled, and normal operation is resumed.

Application Information

SELECTION OF EXTERNAL COMPONENTS

Selection of external components is illustrated through a design example. The design example specifications are as follows:

Buck Converter Design Specifications	
Input voltage range	12.5V to 95V
Output voltage	10V
Maximum Load current	500mA
Switching Frequency	200kHz

RFB1, RFB2:

$V_{OUT} = V_{FB}$ x (R_{FB2}/R_{FB1} + 1), and since V_{FB} = 1.225V, the ratio of R_{FB2} to R_{FB1} calculates as 7:1. Standard values of 6.98kΩ and 1.00kΩ are chosen. Other values could be used as long as the 7:1 ratio is maintained.

Frequency Selection:

At the minimum input voltage, the maximum switching frequency of LM5017 is restricted by the forced minimum off-time ($T_{OFF(MIN)}$) as given by:

$$f_{SW(MAX)} = \frac{1 - D_{MAX}}{T_{OFF(MIN)}} = \frac{1 - 10/12.5}{200\ ns} = 1\ MHz$$

Similarly, at maximum input voltage, the maximum switching frequency of LM5017 is restricted by the minimum T_{ON} as given by:

$$f_{SW(MAX)} = \frac{D_{MIN}}{T_{ON(MIN)}} = \frac{10/95}{100\ ns} = 1.05\ MHz$$

Resistor R_{ON} sets the nominal switching frequency based on the following equations:

$$f_{SW} = \frac{V_{OUT}}{K \times R_{ON}}$$

where K = 1 x 10^{-10}. Operation at high switching frequency results in lower efficiency while providing the smallest solution. For this example a conservative 200kHz was selected, resulting in R_{ON} = 504kΩ. Selecting a standard value for R_{ON} = 499kΩ results in a nominal frequency of 202kHz.

Inductor Selection:

The minimum inductance is selected to limit the output ripple to 20 to 40 percent of the maximum load current. In addition, the peak inductor current at maximum load should be smaller than the minimum current limit as given in electrical characteristics table. The inductor current ripple is given by:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L1 \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

The maximum ripple is observed at maximum input voltage. Substituting V_{IN} = 95V and Δ_{IL} = 40 percent x $I_{OUT\ (max)}$ results in L1 = 198.4µH. The next higher standard value of 220µH is chosen. The peak-to-peak minimum and maximum inductor current ripples of 35mA and 204mA are given at minimum and maximum input voltages respectively. The peak inductor and switch current is given by

$$I_{LI}(peak) = I_{OUT} + \frac{\Delta I_{L(MAX)}}{2} = 602\ mA$$

which is smaller than the minimum current limit. The inductor should be able to withstand the maximum current limit of 1.3A, which can be reached during startup and overload conditions.

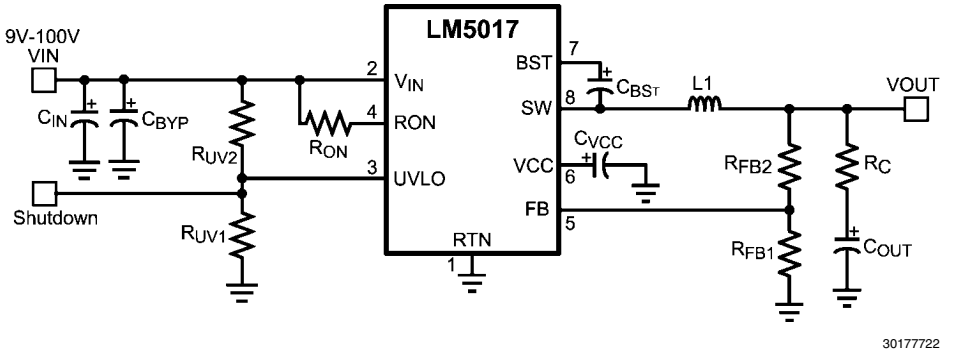


FIGURE 5. Reference Schematic for Selection of External Components

Output Capacitor:

The output capacitor is selected to minimize the capacitive ripple across it. The maximum ripple is observed at maximum input voltage and is given by:

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{sw} \times \Delta V_{ripple}}$$

where ΔV_{ripple} is the voltage ripple across the capacitor. Substituting ΔV_{ripple} = 10mV gives C_{OUT} = 12.64µF. A 22µF standard value is selected. An X5R or X7R type capacitor with a voltage rating 16V or higher should be selected.

Series Ripple Resistor R_C:

The series resistor should be selected to produce sufficient ripple at the feedback node. The ripple produced by R_C is proportional to the inductor current ripple, and therefore R_C should be chosen for minimum inductor current ripple which occurs at minimum input voltage. The R_C is calculated by the equation:

$$R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}} \times \frac{V_{OUT}}{V_{REF}}$$

This gives an R_C of greater than or equal to 5.15Ω. Selecting R_C = 5.23Ω results in ~1V of maximum output voltage ripple. For applications requiring lower output voltage ripple, Type II or Type III ripple injection circuits should be used as described in the section "Ripple Configuration".

V_{CC} and Bootstrap Capacitor:

The V_{CC} capacitor provides charge to bootstrap capacitor as well as internal circuitry and low side gate driver. The Bootstrap capacitor provides charge to high side gate driver. A good value for CV_{CC} is 1µF. A good value for C_{BST} is 0.01µF.

Input Capacitor:

Input capacitor should be large enough to limit the input voltage ripple:

$$C_{IN} \geq \frac{I_{OUT(MAX)}}{8 \times f_{SW} \times \Delta V_{IN}}$$

choosing a ΔV_{IN} = 0.5V gives a minimum C_{IN} = 1.24µF. A standard value of 2.2µF is selected. The input capacitor should be rated for the maximum input voltage under all conditions. A 100V, X7R dielectric should be selected for this design.

Input capacitor should be placed directly across V_{IN} and RTN (pin 2 and 1) of the IC. If it is not possible to place all of the input capacitor close to the IC, a 0.47µF capacitor should be placed near the IC to provide a bypass path for the high frequency component of the switching current. This helps limit the switching noise.

UVLO Resistors:

The UVLO resistors R_{FB1} and R_{FB2} set the UVLO threshold and hysteresis according to the following relationship:

$$V_{IN}(HYS) = I_{HYS} \times R_{UV2}$$

and

$$V_{IN}\,(UVLO,rising) = 1.225V \times \left(\frac{R_{UV2}}{R_{UV1}} + 1\right)$$

where I_{HYS} = 20µA. Setting UVLO hysteresis of 2.5V and UVLO rising threshold of 12V results in R_{UV1} = 14.53kΩ and R_{UV2} = 125kΩ. Selecting standard value of R_{UV1} = 14kΩ and R_{UV2} = 125kΩ results in UVLO thresholds and hysteresis of 12.4V and 2.5V respectively.

APPLICATION CIRCUIT: 12V TO 95V INPUT AND 10V, 500mA OUTPUT BUCK CONVERTER

The application schematic of a buck supply is shown in *Figure 6* below. For output voltage (V_{OUT}) above the maximum regulation threshold of V_{CC} (8.55V, see electrical characteristics), the V_{CC} pin can be connected to V_{OUT} through a diode (D2), as shown below, for higher efficiency and lower power dissipation in the IC.

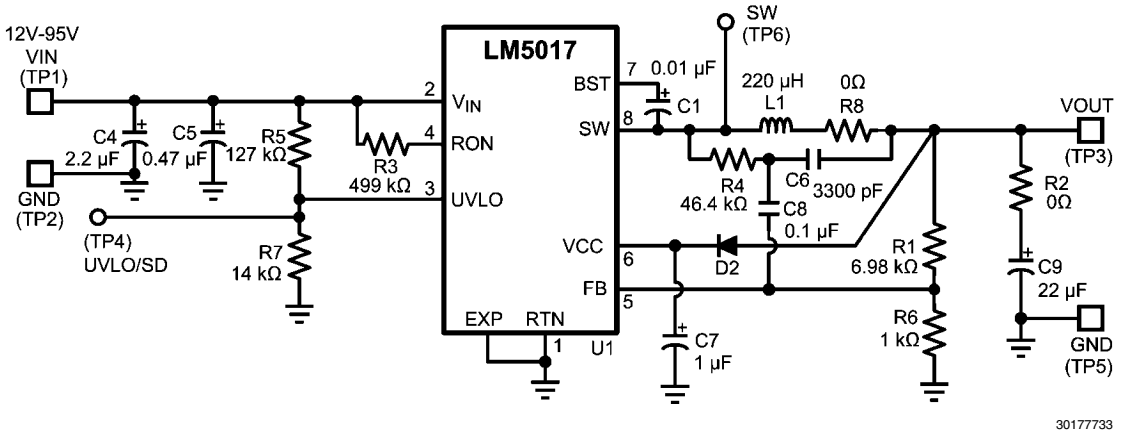


FIGURE 6. Final Schematic for 12V to 95V Input, and 10V, 500mA Output Buck Converter

ISOLATED DC-DC CONVERTER USING LM5017

An isolated supply using LM5017 is shown in *Figure 7* below. Inductor (L) in a typical buck circuit is replaced with a coupled inductor (X1). A diode (D1) is used to rectify the voltage on a secondary output. The nominal voltage at the secondary output (V_{OUT2}) is given by:

$$V_{OUT2} = V_{OUT1} \times \frac{N_S}{N_P} - V_F$$

where VF is the forward voltage drop of D1, and NP, NS are the number of turns on the primary and secondary of coupled inductor X1. For output voltage (V_{OUT1}) above the maximum V_{CC} (8.55V), the V_{CC} pin can be diode connected to V_{OUT1} for higher effiicency and low dissipation in the IC. See AN-2204 for a complete isolated bias design with LM5017.

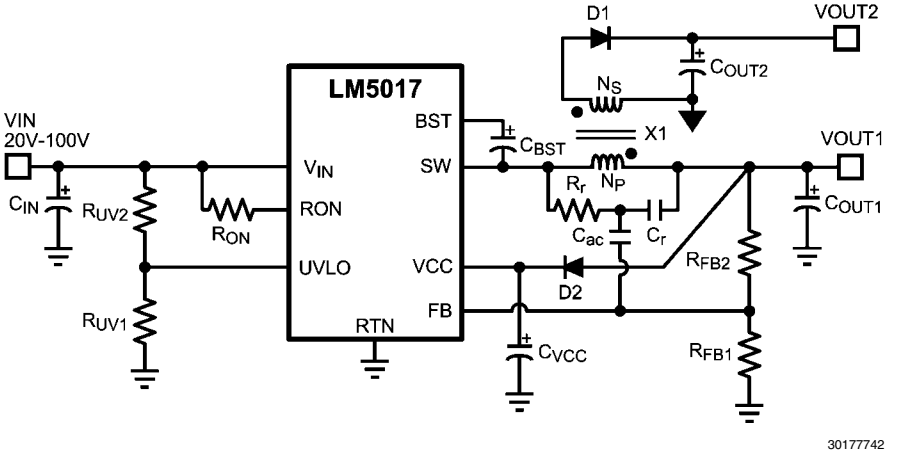


FIGURE 7. Typical Isolated Application Schematic

RIPPLE CONFIGURATION

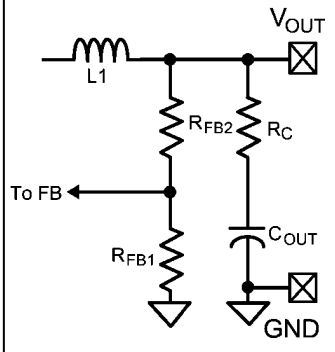
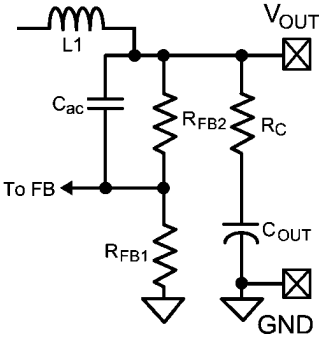
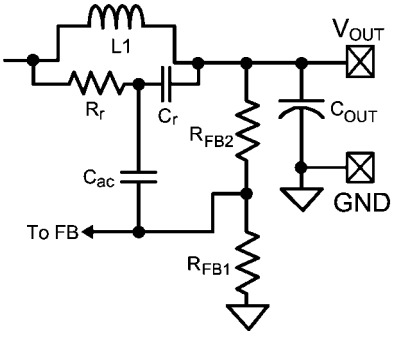
LM5017 uses Constant-On-Time (COT) control scheme, in which the on-time is terminated by an on-timer, and the off-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage (V_{REF}). Therefore, for stable operation, the feedback voltage must decrease monotonically, in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage (V_{FB}) during off-time must be large enough to suppress any noise component present at the feedback node.

Table 1 shows three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple at the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging/discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor.

The capacitive ripple is not in phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at the output node (V_{OUT}) for stable operation. If this condition is not satisfied unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off-time.

Type 3 ripple method uses R_r and C_r and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is ac coupled using C_{ac} to the feedback node (FB). Since this circuit does not use the output voltage ripple, it is ideally suited for applications where low output voltage ripple is required. See application note AN-1481 for more details for each ripple generation method.

Type 1 Lowest Cost Configuration	Type 2 Reduced Ripple Configuration	Type 3 Minimum Ripple Configuration
		
$R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}} \times \frac{V_{OUT}}{V_{REF}}$	$C \geq \frac{5}{f_{sw}(R_{FB2} \| R_{FB1})}$ $R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}}$	$C_r = 3300\ pF$ $C_{ac} = 100\ nF$ $R_r C_r \leq \frac{(V_{IN(MIN)} - V_{OUT}) \times T_{ON}}{25\ mV}$

SOFT START

A soft-start feature can be implemented to the LM5017 using an external circuit. As shown in *Figure 8*, the soft-start circuit consists of one capacitor, C_1, two resistors, R_1 and R_2, and a diode, D. During the initial start-up, the VCC voltage is established prior to the V_{OUT} voltage. D is thereby forward biased and the FB voltage is pulled up above the reference voltage (1.225V). The switcher is disabled. With the charging of the capacitor C_1, the voltage at node B gradually decreases. Due to the action of the control circuit, V_{OUT} will gradually rise to maintain the FB voltage at the reference voltage. Once the voltage at node B is lower than the FB voltage, plus the voltage drop of D, the soft-start is finished and D is reverse biased.

During the initial part of the start-up, the FB voltage can be approximated as follows. Please note that the effect of R_1 has been ignored to simplify the calculation:

$$V_{FB} = (VCC - V_D) \times \frac{R_{FB1} \times R_{FB2}}{R_2 \times (R_{FB1} + R_{FB2}) + R_{FB1} \times R_{FB2}}$$

To achieve the desired soft-start, the following design guidance is recommended:

(1) R_2 is selected so that V_{FB} is higher than 1.225V for a V_{CC} of 4.5V, but is lower than 5V when V_{CC} is 8.55V. If an external V_{CC} is used, V_{FB} should not exceed 5V at maximum V_{CC}.

(2) C_1 is selected to achieve the desired start-up time that can be determined as follows:

$$t_S = C_1 \times (R_2 + \frac{R_{FB1} \times R_{FB2}}{R_{FB1} + R_{FB2}})$$

(3) R_1 is used to maintain the node B voltage at zero after the soft-start is finished. A value larger than the feedback resistor divider is preferred.

Based on the schematic shown in *Figure 6*, selecting C_1=1uF, R_2=1kΩ, R_1=30kΩ results in a soft-start time of about 2ms.

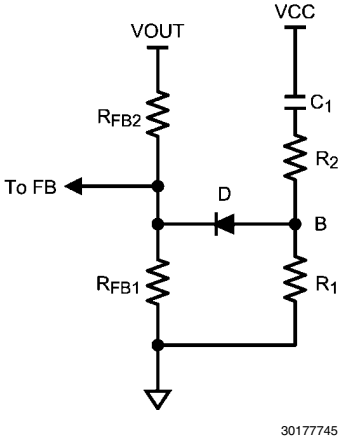


FIGURE 8. Soft-Start Circuit

LAYOUT RECOMMENDATION

A proper layout is essential for optimum performance of the circuit. In particular, the following guidelines should be observed:

1. C_{IN}: The loop consisting of input capacitor (C_{IN}), V_{IN} pin, and RTN pin carries switching currents. Therefore, the input capacitor should be placed close to the IC, directly across V_{IN} and RTN pins and the connections to these two pins should be direct to minimize the loop area. In general it is not possible to accommodate all of input capacitance near the IC. A good practice is to use a 0.1µF or 0.47µF capacitor directly across the V_{IN} and RTN pins close to the IC, and the remaining bulk capacitor as close as possible (Refer to *Figure 9* Placement of Bypass Capacitors).
2. C_{VCC} and C_{BST}: The V_{CC} and bootstrap (BST) bypass capacitors supply switching currents to the high and low side gate drivers. These two capacitors should also be placed as close to the IC as possible, and the connecting trace length and loop area should be minimized (See *Figure 9* Placement of Bypass Capacitors).
3. The Feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of LM5017. Therefore, care should be taken while routing the feedback trace to avoid coupling any noise to this pin. In particular, feedback trace should not run close to magnetic components, or parallel to any other switching trace.
4. SW trace: The SW node switches rapidly between V_{IN} and GND every cycle and is therefore a possible source of noise. The SW node area should be minimized. In particular, the SW node should not be inadvertently connected to a copper plane or pour.

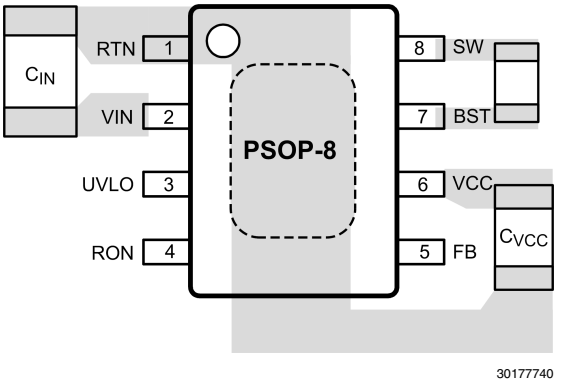
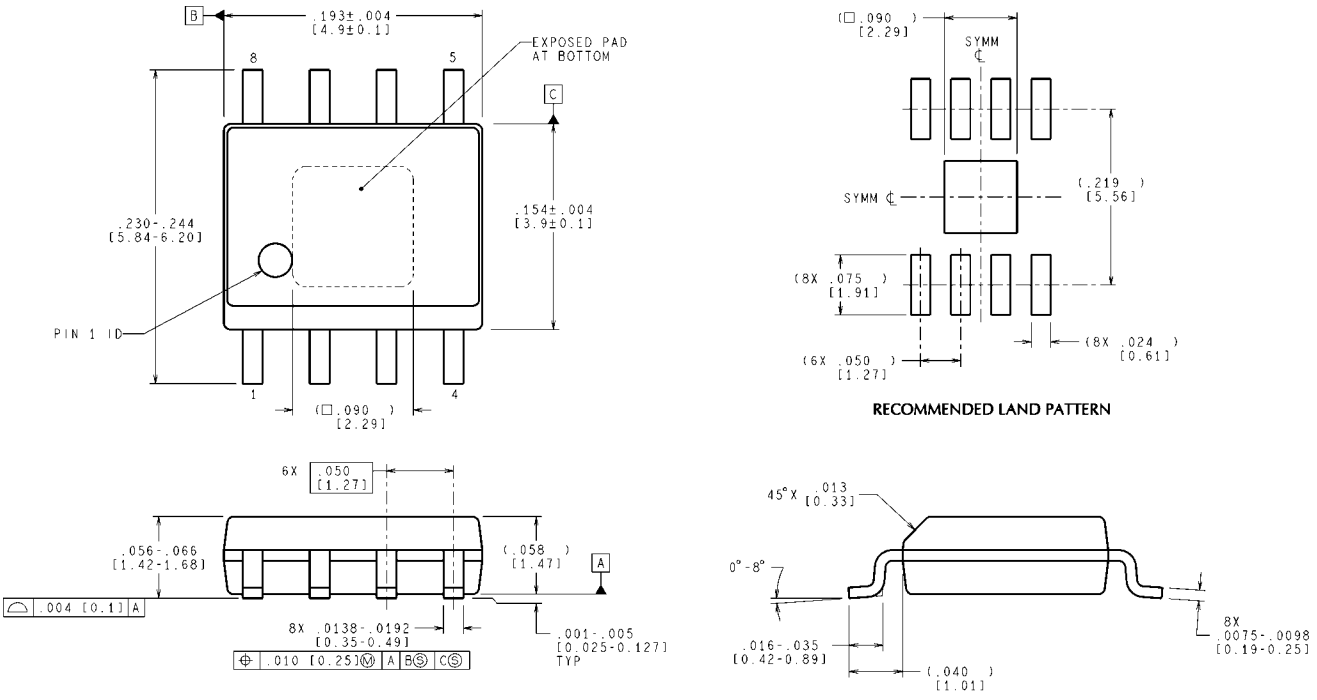


FIGURE 9. Placement of Bypass Capacitors

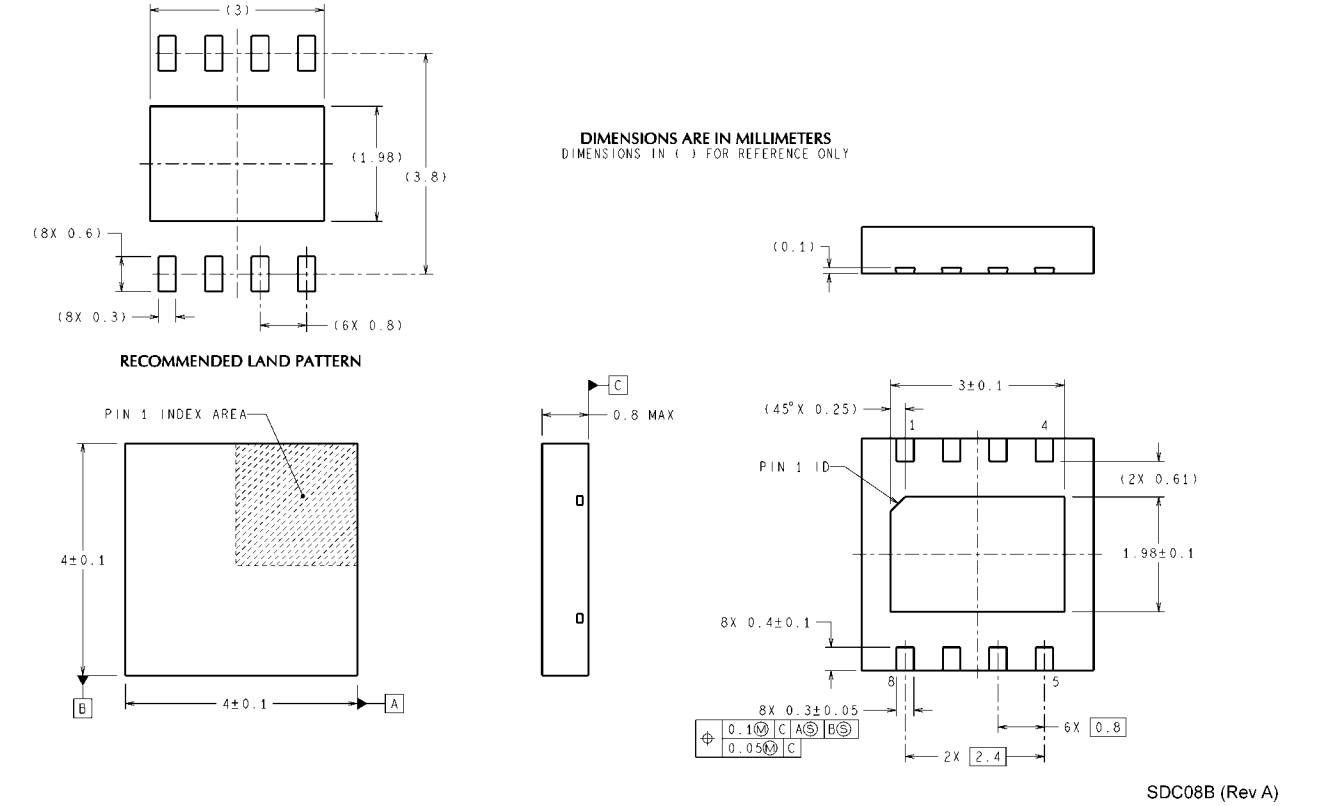
Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MRA08A (Rev D)

PSOP–8 Outline Drawing
NS Package Number MRA08A



SDC08B (Rev A)

8-Lead LLP Package
NS Package Number SDC08B

Notes