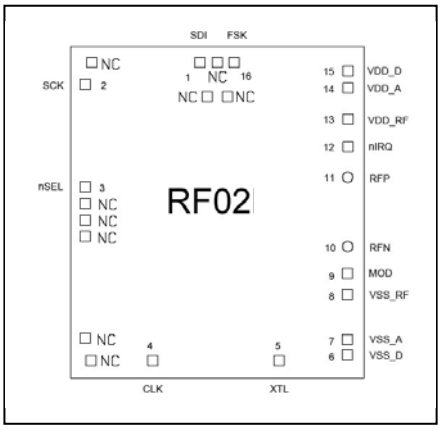
RF02 Universal ISM Band FSK Transmitter

RF02



DESCRIPTION

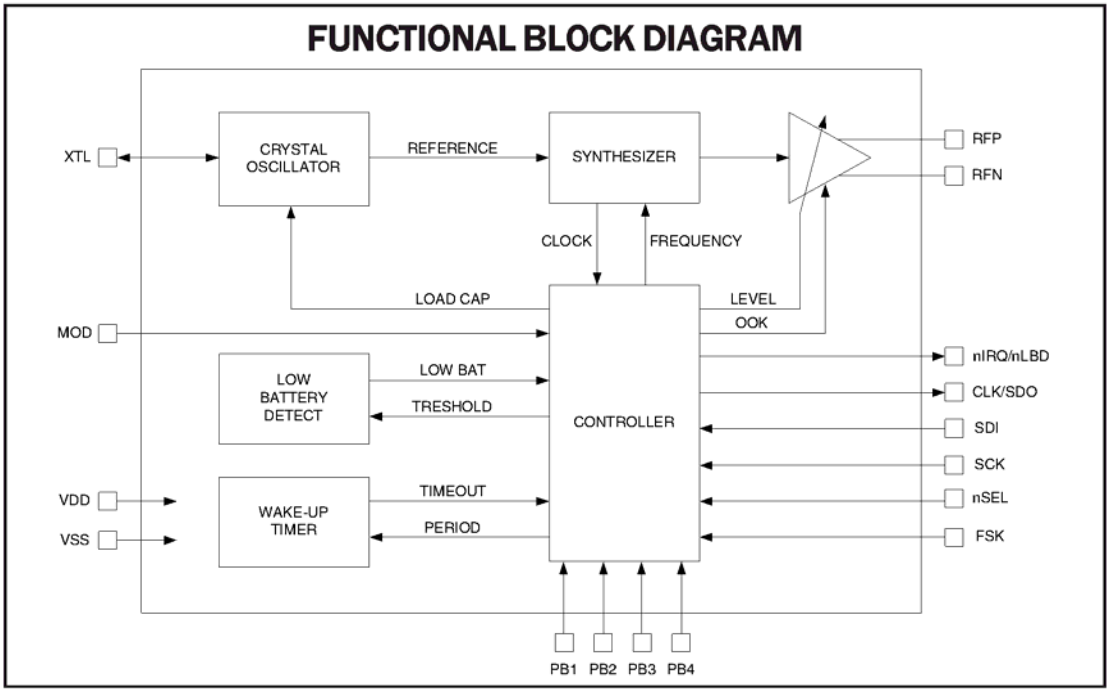
Hope's RF02 is a single chip, low power, multi-channel FSK transmitter designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 433, 868, and 915 MHz bands. Used in conjunction with RF01, Hope's FSK receiver, the RF02 transmitter produces a flexible, low cost, and highly integrated solution that does not require production alignments. All required RF functions are integrated. Only an external crystal and bypass filtering are needed for operation. The RF02 offering a higher output power and an improved phase noise characteristic.

The RF02 features a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency hopping, bypassing multipath fading and interference to achieve robust wireless links. In addition, highly stable and accurate FSK modulation is accomplished by direct closed-loop modulation with bit rates up to 115.2 kbps. The PLL's high resolution allows the use of multiple channels in any of the bands.

The integrated power amplifier of the transmitter has an open-collector differential output that directly drive a loop antenna with programmable output level. No additional matching network is required. An automatic antenna tuning circuit is built in to avoid costly trimming procedures and de-tuning due to the "hand effect".

For low-power applications, the device supports automatic activation from sleep mode. Active mode can be initiated by several wake-up events (on-chip timer timeout, low supply voltage detection).

FUNCTIONAL BLOCK DIAGRAM



FEATURES

- Fully integrated (low BOM, easy design-in)
- No alignment required in production
- Fast settling, programmable, high-resolution PLL
- Fast frequency hopping capability
- Stable and accurate FSK modulation with programmable deviation
- Programmable PLL loop bandwidth
- Direct loop antenna drive
- Automatic antenna tuning circuit
- Programmable output power level
- SPI bus for applications with microcontroller
- Clock output for microcontroller
- Integrated programmable crystal load capacitor
- Multiple event handling options for wake-up activation
- Wake-up timer
- Low battery detection
- 2.2V to 5.4V supply voltage
- Low power consumption
- Low standby current (0.3 μA)
- Transmit bit synchronization

TYPICAL APPLICATIONS

- Remote control
- Home security and alarm
- Wireless keyboard/mouse and other PC peripherals
- Toy control
- Remote keyless entry
- Tire pressure monitoring
- Telemetry
- Personal/patient data logging
- Remote automatic meter reading

DETAILED FEATURE-LEVEL DESCRIPTION

The RF02 FSK transmitter is designed to cover the unlicensed frequency bands at 433, 868, and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

PLL

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows the usage of multiple channels in any of the bands. The FSK deviation is selectable (from 30 to 210 kHz with 30 kHz increments) to accommodate various bandwidth, data rate and crystal tolerance requirements, and it is also highly accurate due to the direct closed-loop modulation of the PLL. The transmitted digital data can be sent asynchronously through the FSK pin or over the control interface using the appropriate command.

RF Power Amplifier (PA)

The power amplifier has an open-collector differential output and can directly drive a loop antenna with a programmable output power level. An automatic antenna tuning circuit is built in to avoid costly trimming procedures and the so-called "hand effect."

Crystal Oscillator

The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet.

The transmitters can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal. When the chip receives a Sleep Command from the microcontroller and turns itself off, it provides several further clock pulses ("clock tail") for the microcontroller to be able to go to idle or sleep mode. The length of the clock tail is programmable.

Low Battery Voltage Detector

The low battery voltage detector circuit monitors the supply voltage and generates an interrupt if it falls below a programmable threshold level.

Wake-Up Timer

The wake-up timer has very low current consumption (1.5 uA typical) and can be programmed from 1 ms to several days with an accuracy of ±5%.

It calibrates itself to the crystal oscillator at every startup, and then every 30 seconds. When the oscillator is switched off, the calibration circuit switches on the crystal oscillator only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing.

Event Handling

In order to minimize current consumption, the device supports sleep mode. Active mode can be initiated by several wake-up events: timeout of wake-up timer, detection of low supply voltage or through the serial interface.

If any wake-up event occurs, the wake-up logic generates an interrupt, which can be used to wake

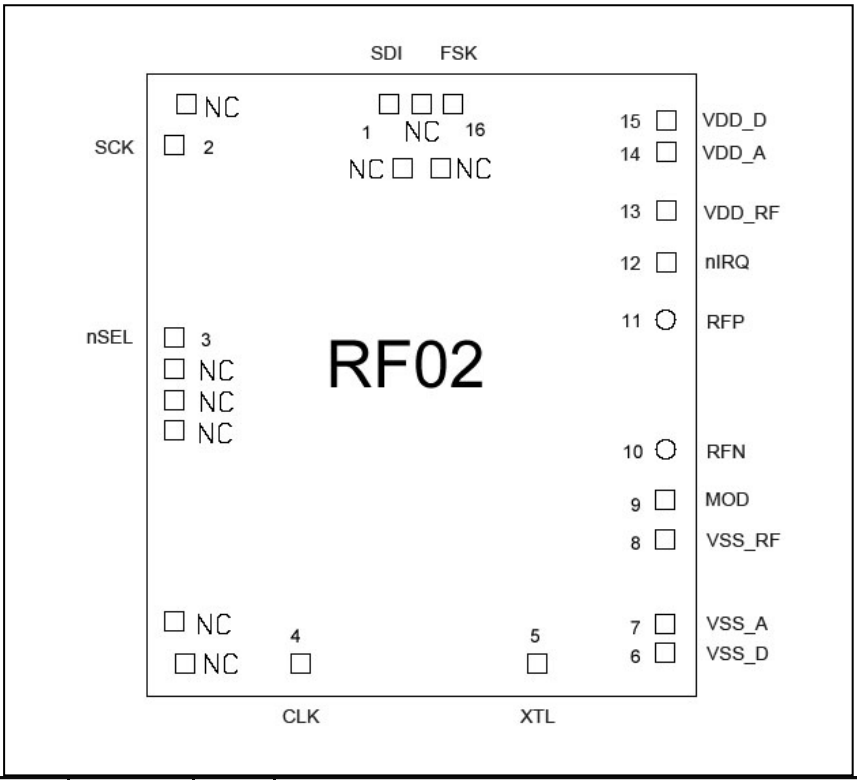
up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the transmitters by the microcontroller through the nIRQ pin.

Interface

An SPI compatible serial interface lets the user select the operating frequency band and center frequency of the synthesizer, polarity and deviation of FSK modulation, and output power level. Division ratio for the microcontroller clock, wake-up timer period, and low battery detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode.

PACKAGE PIN DEFINITIONS

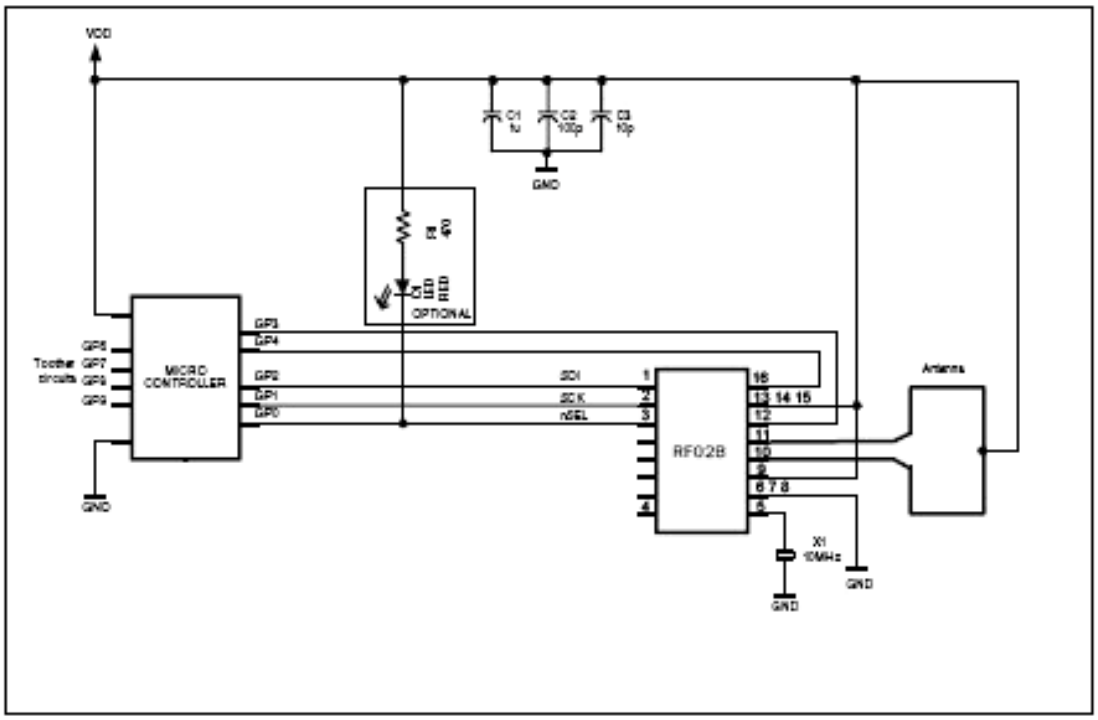
Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output



PinP	Name	Type	Function
1	SDI	DI	Data input of serial control interface
2	SCK	DI	Clock input of serial control interface
3	nSEL	DI	Chip select input of serial control interface (active low)
4	CLK	DO	Microcontroller clock (1 MHz-10 MHz)
5	XTL	AIO	Crystal connection (other terminal of crystal to VSS)
6	VSS_D	S	Digital VSS(Connect to VSS)
7	VSS_A	S	Analog VSS(Connect to VSS)
8	VSS_RF	S	RF VSS(Connect to VSS)

9	MOD	DI	Connect to logic high
10	RFN	AO	Power amplifier output (open collector)
11	RFP	AO	Power amplifier output (open collector)
12	nIRQ	DO	Interrupt request output for microcontroller (active low) and status read output
13	VDD_RF	S	RF VDD(Connect to VDD)
14	VDD_A	S	Analog VDD(Connect to VDD)
15	VDD_D	S	Digital VDD(Connect to VDD)
16	FSK	DI	Serial data input for FSK modulation

Typical application



GENERAL DEVICE SPECIFICATION

All voltages are referenced to V_{ss}, the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	-0.5	6.0	V
V_{in}	Voltage on any pin except open collector outputs	-0.5	V_{dd}+0.5	V
V_{oc}	Voltage on open collector outputs	-0.5	6.0	V
I_{in}	Input current into any pin except VDD and VSS	-25	25	mA
ESD	Electrostatic discharge with human body model		1000	V
T_{st}	Storage temperature	-55	125	℃

Recommended Operating Range

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	2.2	5.4	V
V_{oc}	Voltage on open collector outputs (Max 6.0 V)	V_{dd} - 1	V_{dd} + 1	V
T_{op}	Ambient operating temperature	-40	85	℃

ELECTRICAL SPECIFICATION

(Min/max values are valid over the whole recommended operating range, typ conditions:
T_{op} =27℃;V_{dd} =V_{oc}=2.7V)

DC Characteristics

Symbol	Parameter		Conditions/Notes	Min	Typ	Max	Units
$I_{dd\_TX\_0}$	Supply current (TX mode, Pout =0dBm)	433 MHz band 868 MHz band 915 MHz band	Active state with 0dBm output power		12 14 15		mA
$I_{dd\_TX\_PMAX}$	Supply current (TX mode, Pout =P_{max})	433 MHz band 868 MHz band 915 MHz band	Active state with maximum output power		21 23 24		mA
I_{pd}	Standby current in sleep mode (Note 1)		All blocks disabled		0.3		μA
I_{wt}	Wake-up timer current consumption				1.5		μA
I_{lb}	Low battery detector current consumption				0.5		μA
I_x	Idle current		Only crystal oscillator is on		1.5		mA

V_{lba}	Low battery detection accuracy			+/-3		%
V_{lb}	Low battery detector threshold	Programmable in 0.1 V steps	2.2		5.3	V
V_{il}	Digital input low level				0.3*V_{dd}	V
V_{ih}	Digital input high level		0.7*V_{dd}			V
I_{il}	Digital input current	V_{il} = 0 V	-1		1	µA
I_{ih}	Digital input current	V_{ih} = V_{dd}, V_{dd} = 5.4 V	-1		1	µA
V_{ol}	Digital output low level	I_{ol} = 2 mA			0.4	V
V_{oh}	Digital output high level	I_{oh} = -2 mA	V_{dd}-0.4			V

AC Characteristic

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{ref}	PLL reference frequency	Crystal operation mode is parallel (Note 2)	9	10	11	MHz
f_o		433MHz band, 2.5kHz resolution 868MHz band, 5.0kHz resolution 915MHz band, 7.5kHz resolution	430.24 860.48 900.72		439.75 879.51 929.27	MHz
t_{lock}	PLL lock time	Frequency error < 10 kHz after 10 MHz step, POR default PLL setting(Note 7)		20		µs
t_{sp}	PLL startup time	After turning on from idle mode, with crystal oscillator already stable, POR default PLL setting (Note 7)			250	µs
I_{OUT}	Open collector output current (Note 3)	At all bands	0.5		6	mA
P_{maxL}	Available output power (433MHz band)	With opt. antenna impedance (Note 4)		8		dBm
P_{maxH}	Available output power (868 and 915 MHz band)	With opt. antenna impedance (Note 4)		6		dBm
P_{out}	Typical output power	Selectable in 3 dB steps (Note 3)	P_{max}-21		P_{max}	dBm
P_{sp}	Spurious emission	At max power with loop antenna (Note 5)			-50	dBc

C_o	Output capacitance (set by the automatic antenna tuning circuit)	At low bands At high bands	1.5 1.6	2.3 2.2	2.8 3.1	pF
Q_o	Quality factor of the output capacitance		16	18	22	pF
L_{out}	Output phase noise	100 kHz from carrier 1 MHz from carrier (Note 7)		-85 -105		dBc/Hz
BR_{FSK}	FSK bit rate	(Note 7)			115.2	kbps
df_{fsk}	FSK frequency deviation	Programmable in 30 kHz steps	30		210	kHz
C_{xl}	Crystal load capacitance See Crystal Selection Guidelines	Programmable in 0.5 pF steps, tolerance +/-10%	8.5		16	pF
t_{POR}	Internal POR timeout (Note 6)	After V_{dd} has reached 90% of final value			50	ms
t_{sx}	Crystal oscillator startup time	Crystal ESR < 100 Ohms		1.5	5	ms
t_{PBt}	Wake-up timer clock period	Calibrated every 30 seconds	0.95		1.05	ms
$t_{wake-up}$	Programmable wake-up time		1		$5 *10^{11}$	ms
$C_{in, D}$	Digital input capacitance				2	pF
$t_{r, f}$	Digital output rise/fall time	15 pF pure capacitive load			10	ns

Note 1: Using a CR2032 battery (225 mAh capacity), the expected battery life is greater than 2 years using a 60-second wake-up period for sending 50 byte packets in length at 19.2 kbps with +6 dBm output power in the 915 MHz band.

Note 2: Using anything but a 10 MHz crystal is allowed but not recommended because all crystal-referred timing and frequency parameters will change accordingly.

Note 3: Adjustable in 8 steps.

Note 4: Optimal antenna admittance/impedance for the RF02:

	Yantenna [S]	Zantenna [Ohm]	Lantenna [nH]
434 MHz	1.3E-3 - j6.3E-3	31 + j152	58.00
868 MHz	1.35E-3 - j1.2E-2	9 + j82	15.20
915 MHz	1.45E-3 - j1.3E-2	8.7 + j77	13.60

Note 5: With selective resonant antennas .

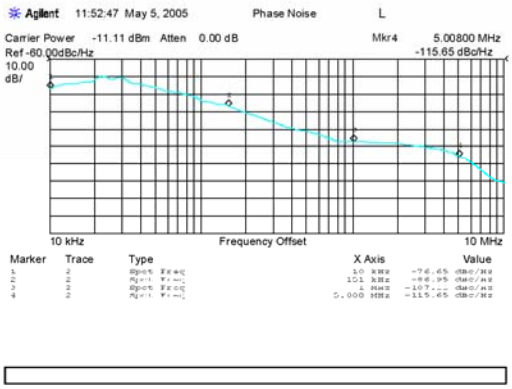
Note 6: During this period, no commands are accepted by the chip.

Note 7: The maximum FSK bitrate and the Output phase noise are dependent on the actual setting of the PLL Setting Command.

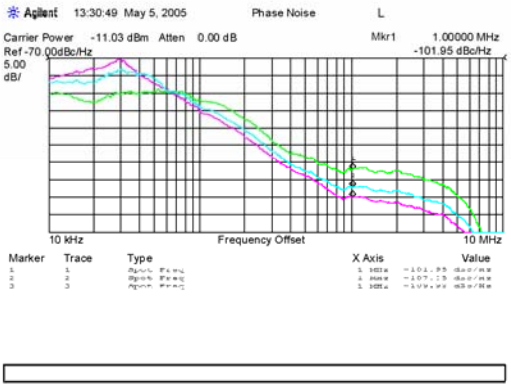
TYPICAL PERFORMANCE DATA (RF02)

Phase noise measurements in the 868 MHz ISM band

50% Charge pump current setting
(Ref. level: -60 dBc/Hz, 10 dB/div)



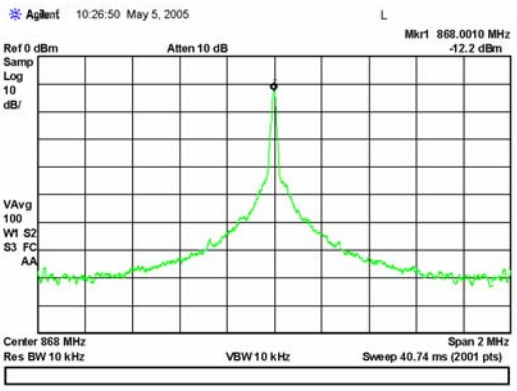
100, 50, 33% Charge pump current settings
(Ref. level: -70 dBc/Hz, 5 dB/div)



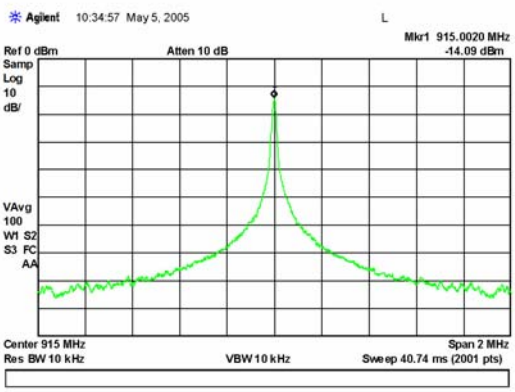
Unmodulated RF Spectrum

The output spectrum is measured at different frequencies. The output is loaded with 50 Ohms through a matching network.

At 868 MHz

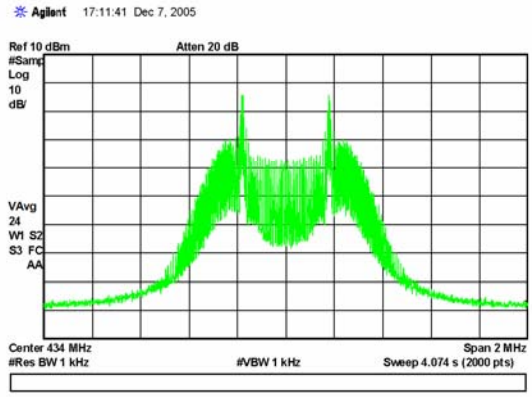


At 915 MHz

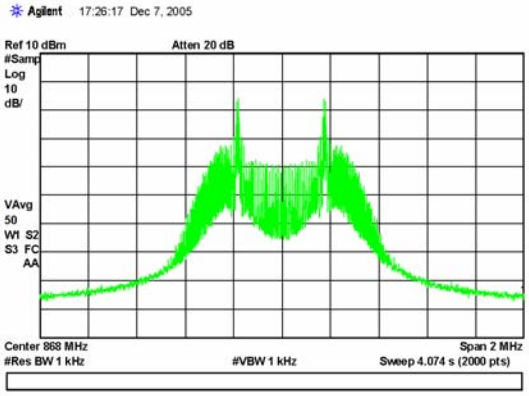


Modulated RF Spectrum

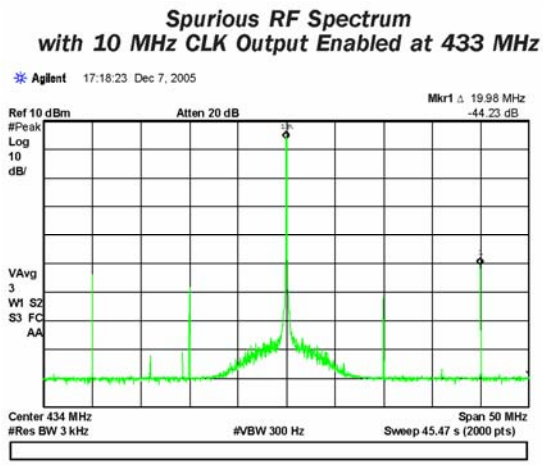
At 433 MHz with
180 kHz Deviation at 9.6 kbps

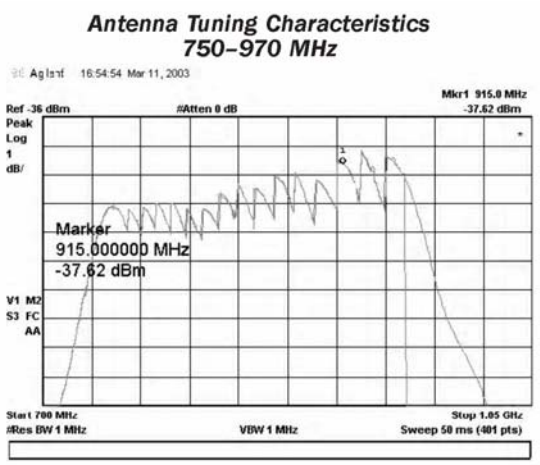


At 868 MHz with
180 kHz Deviation at 9.6 kbps



Other Important Characteristics





The antenna tuning characteristics was recorded in “max-hold” state of the spectrum analyzer. During the measurement, the transmitters were forced to change frequencies by forcing an external reference signal to the XTL pin. While the carrier was changing the antenna tuning circuit switched trough all the available states of the tuning circuit. The graph clearly demonstrates that while the complete output circuit had about a 40 MHz bandwidth, the tuning allows operating in a 220 MHz band. In other words the tuning circuit can compensate for 25% variation in the resonant frequency due to any process or manufacturing spread.

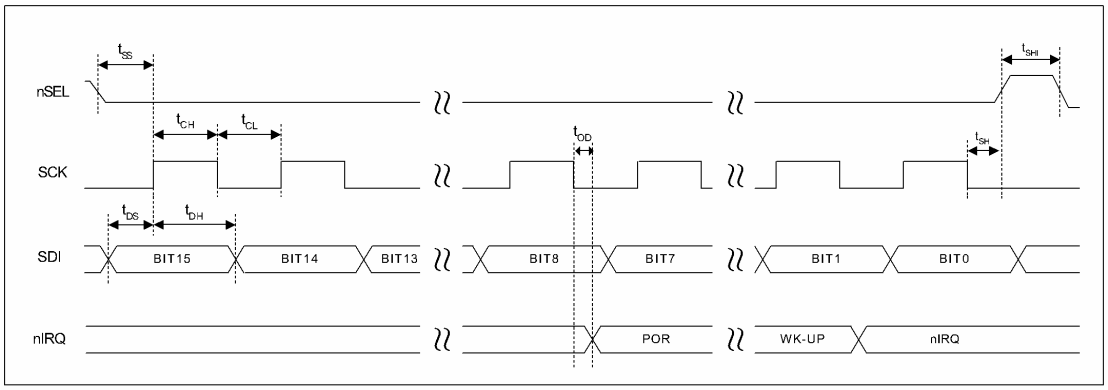
CONTROL INTERFACE

Commands to the transmitters are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don’t care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control and command registers.

Timing Specification

Symbol	Parameter	Minimum Value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10

Timing Diagram



Control Commands

	Control Command	Related Parameters/Functions
1	Configuration Setting Command	Frequency band, microcontroller clock output, crystal load capacitance, frequency deviation
2	Power Management Command	Crystal oscillator, synthesizer, power amplifier, low battery detector, wake-up timer, clock output buffer
3	Frequency Setting Command	Carrier frequency
4	Data Rate Command	Bit rate
5	Power Setting Command	Nominal output power, OOK mode
6	Low Battery Detector Command	Low battery threshold limit
7	Sleep Command	Length of the clock tail after power down
8	Wake-Up Timer Command	Wake-up time period
9	Data Transmit Command	Data transmission
10	Status Register Command	Transmitter status read
11	PLL Setting Command	PLL bandwidth can be modified by this command

Note: In the following tables the POR column shows the default values of the command registers after power-on.

1. Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	b1	b0	d2	d1	d0	x3	x2	x1	x0	ms	m2	m1	m0	8080h

b1	b0	Frequency Band [MHz]
0	1	433
1	0	868
1	1	915

x3	x2	x1	x0	Crystal Load Capacitance [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
……				……
1	1	1	0	15.5

d2	d1	d0	Clock Output Frequency [MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

The resulting output frequency can be calculated as:

$f_{out} = f0 – (-1)^{SIGN} * (M + 1) * (30\ kHz)$

where:

f0 is the channel center frequency (see the next command)

M is the three bit binary number <m2 : m0>

SIGN = (ms) XOR (FSK input)

Note:

• Use M in a range from 0 to 6.

2. Power Management Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	a1	a0	ex	es	ea	eb	et	dc	C000h

Bits 5-0, enable the corresponding block of the transmitters, i.e. the crystal oscillator is enabled by the ex bit, the synthesizer by es, the power amplifier by ea and the low battery detector by eb, while the wake-up timer by et. The bit dc disables the clock output buffer.

When receiving the Data Transmit Command, the chip supports automatic on/off control over the crystal oscillator, the PLL and the PA.

If bit a1 is set, the crystal oscillator and the synthesizer are controlled automatically. Data Transmit Command starts up the crystal oscillator and as soon as a stable reference frequency is available the synthesizer starts. After a subsequent delay to allow locking of the PLL, if a0 is set the power amplifier is turned on as well.

Note:

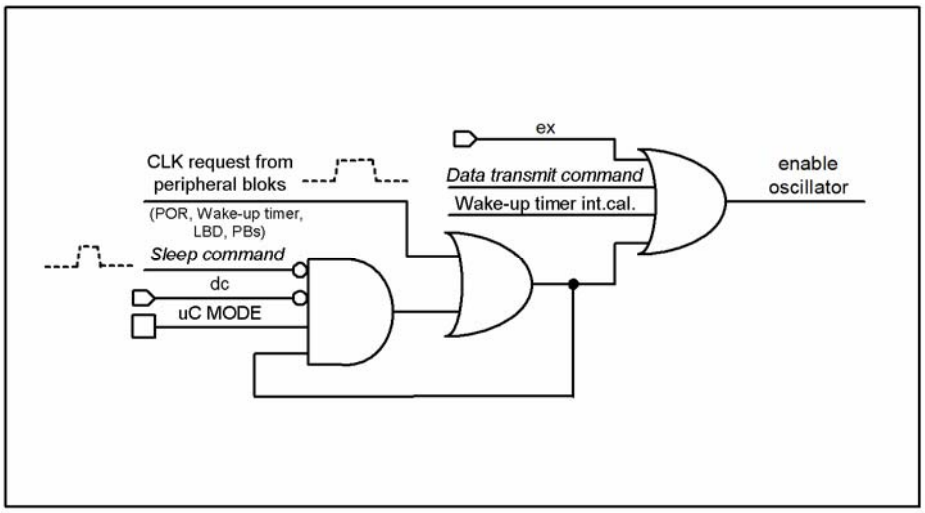
To enable the automatic internal control of the crystal oscillator, the synthesizer and the power amplifier, the corresponding bits (ex, es, ea) must be zero in the Power Management Command.

The ex bit should be set in the Power Management Command for the correct control of es and ea. The oscillator can be switched off by clearing the ex bit after the transmission.

The Sleep Command can be used to indicate the end of the data transmission process.

For processing the events caused by the peripheral blocks (POR, LBD or wake-up timer) the chip requires operation of the crystal oscillator. This operation is fully controlled internally, independently from the status of the ex bit, but if the dc bit is zero, the oscillator remains active until Sleep Command is issued. (This command can be considered as an event controller reset.)

Oscillator control logic



3. Frequency Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A7D0h

The 12-bit parameter of the Frequency Setting Command <f11 : f0> has the value F. The value F should be in the range of 96 and 3903. When F is out of range, the previous value is kept. The synthesizer center frequency f_0 can be calculated as:

f_0 = 10 MHz * C1 * (C2 + F/4000)

The constants C1 and C2 are determined by the selected band as:

Band [MHz]	C1	C2
433	1	43
868	2	43
915	3	30

Note:

• For correct operation of the frequency synthesizer, the frequency and band of operation need to be programmed before the synthesizer is started. Directly after activation of the synthesizer, the RF VCO is calibrated to ensure proper operation in the programmed frequency band.

4. Data Rate Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	r7	r6	r5	r4	r3	r2	r1	r0	C800h

The transmitted bit rate is determined by the 8-bit value R (bits *<r7 : r0>)* as:

BR = 10 MHz / 29 / (R+1)

Apart from setting custom values, the standard bit rates from 2.4 to 115.2 kbps can be approximated with minimal error.

Note:

• PLL bandwidth should be set according the data rate. Please see the *PLL Setting Command*.

5. Power Setting Command

bit	7	6	5	4	3	2	1	0	POR
	1	0	1	1	0	p2	p1	p0	B0h

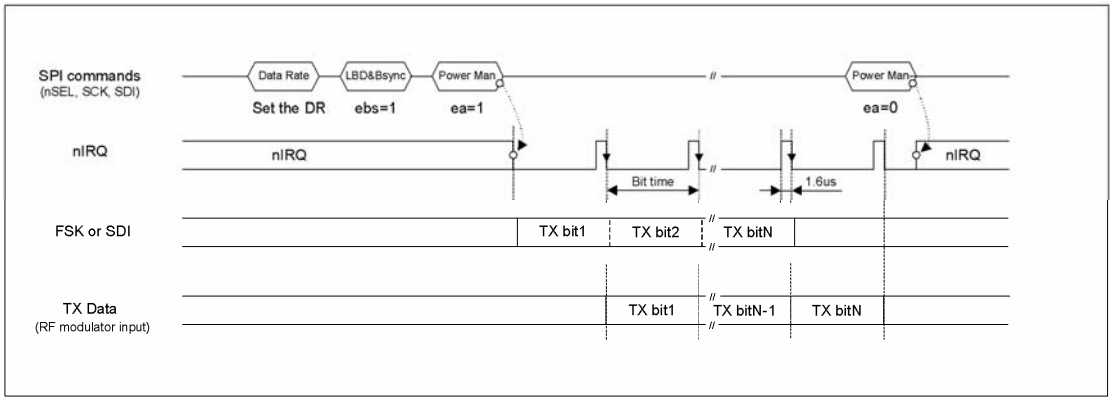
2	p1	p0	Output Power [dB]
0	0	0	0
0	0	1	-3
0	1	0	-6
0	1	1	-9
1	0	0	-12
1	0	1	-15
1	1	0	-18
1	1	1	-21

The output power is given in the table as relative to the maximum available power, which depends on the actual antenna impedance.

6. Low Battery Detector and TX Bit Synchronization Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	dwc	0	ebs	t4	t3	t2	t1	t0	C200h

Bit 7 <dwc> Disables the Wake-up timer periodical (every 30 second) calibration if this bit is set.
Bit 5 <ebs> Enables the TX bit synchronization circuit. The data rate must be set by the Data Rate Command.5



The 5-bit value T of <t4 : t0> determines the threshold voltage V_{lb} of the detector:

$$V_{lb} = 2.2\ V + T * 0.1\ V$$

7. Sleep Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0	C400h

The effect of this command depends on the Power Management Command. It immediately disables the power amplifier (if a0=1 and ea=0) and the synthesizer (if a1=1 and es=0). Stops the crystal oscillator

after S periods of the microcontroller clock (if a1=1 and ex=0) to enable the microcontroller to execute all necessary commands before entering sleep mode itself. The 8-bit value S is determined by bits <s7:s0>.

8. Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E000h

The wake-up time period can be calculated as:

$$T_{wake\text{-}up} = M * 2^R \text{ [ms]},$$

where M is defined by the <m7 : m0> digital value and R is defined by the <r4 : r0> digital value.

Note:

- For continual operation the et bit should be cleared and set at the end of every cycle.

9. Data Transmit Command

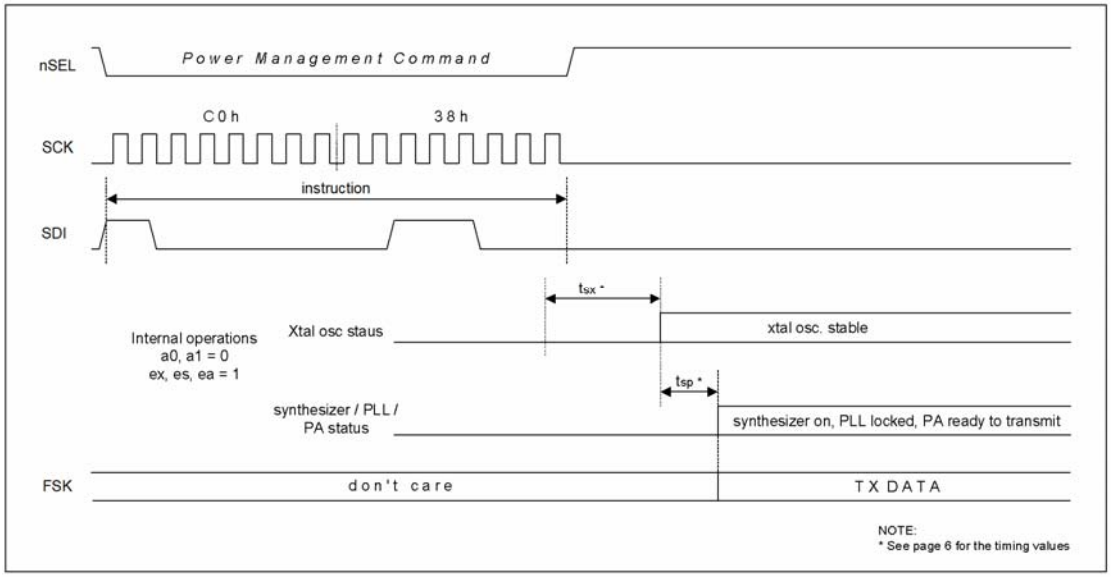
bit	7	6	5	4	3	2	1	0
	1	1	0	0	0	1	1	0

This Command Indicates that the following bitstream coming in via the serial interface is to be transmitted.

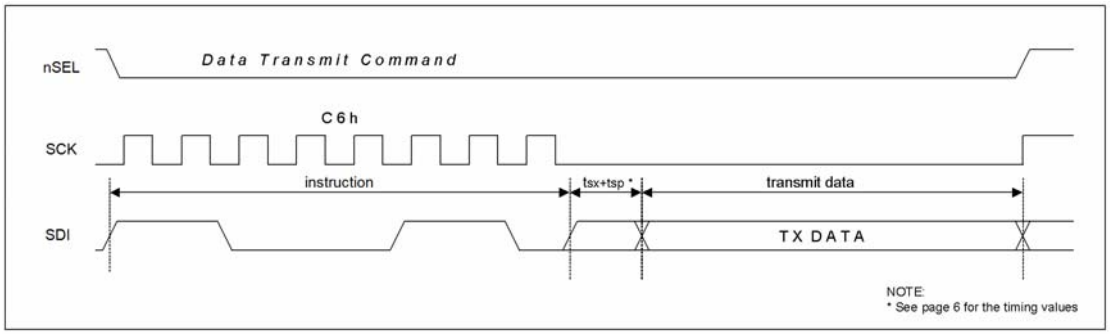
Note

- This command is not needed if the transmitters' power management bits (*ex, es and ea*) are fully controlled by the microcontroller and TX data comes through the FSK pin.
- If the crystal oscillator was formerly switched off (*ex*=0), the internal oscillator needs t_{sx} time, to switch on. The actual value depends on the type of quartz crystal used.
- If the synthesizer was formerly switched off (*es*=0), the internal PLL needs t_{sp} startup time. Valid data can be transmitted only when the internal locking process is finished.

Data Transmit Sequence Through the FSK Pin



Data Transmit Sequence Through the SDI Pin



Note:

Do not send CLK pulses with the TX data bits, otherwise they will be interpreted as commands.

This mode is not SPI compatible.

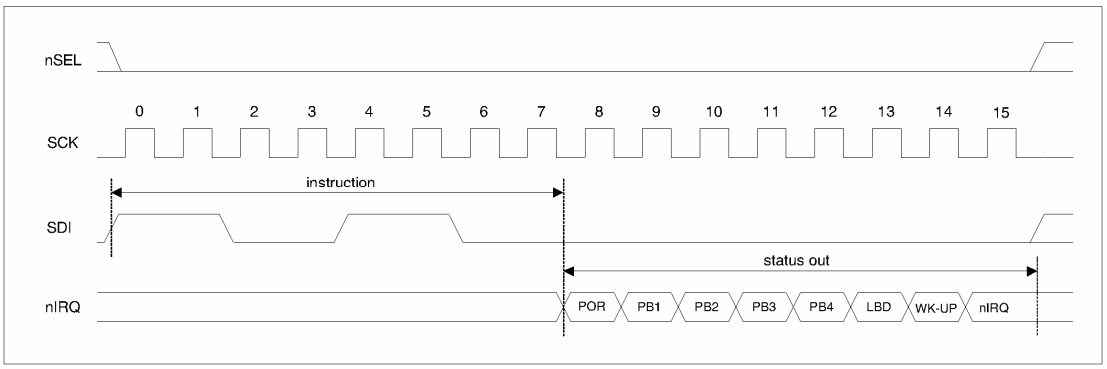
If the crystal oscillator and the PLL are running, the $t_{sx}+t_{sp}$ delay is not needed.

10 . Status Register Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	--

With this command, it is possible to read the chip's status register through the nIRQ pin. This command clears the last serviced interrupt and processing the next pending one will start (if there is any).

Status Register Read Sequence



11. PLL Setting Command

PLL bandwidth can be selected by this command

PLL command	Max data rate [kbps]	Phase noise at 1MHz offset [dbc/Hz]	Comments
D240h	19.2	-112	25%current
D2C0h	38.4	-110	33%current
D200h	68.9	-107	50%current
D280h	115.2	-102	100%current

RX-TX ALIGNMENT PROCEDURES

RX-TX frequency offset can be caused only by the differences in the actual reference frequency. To minimize these errors it is suggested to use the same crystal type and the same PCB layout for the crystal placement on the RX and TX PCBs.

To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the "en" bit in the AFC Control Command (bit 0).

CRYSTAL SELECTION GUIDELINES

The crystal oscillator of the RF02 requires a 10 MHz parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 pF to 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 pF to 20 pF so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF and a worst case 7 pF shunt capacitance (C0) value is expected for the crystal, the oscillator is able to start up with any crystal having less than 100 ohms ESR (equivalent series loss resistance). However, lower C0 and ESR values guarantee faster oscillator startup. It is recommended to keep the PCB parasitic capacitances on the XTL pin as low as possible.

The crystal frequency is used as the reference of the PLL, which generates the RF carrier frequency (fc). Therefore fc is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable carrier frequency error.

Maximum XTAL Tolerances Including Temperature and Aging [ppm]

Bit Rate: 2.4kbps	Transmitter Deviation [+/- kHz]						
	30	60	90	120	150	180	210
315 MHz	30	75	100	100	100	100	100
433 MHz	20	50	75	100	100	100	100
868 MHz	10	25	40	60	75	100	100
915 MHz	10	25	40	50	75	75	100

Bit Rate: 9.6kbps	Transmitter Deviation [+/- kHz]						
	30	60	90	120	150	180	210
315 MHz	25	70	100	100	100	100	100
433 MHz	15	50	75	100	100	100	100
868 MHz	8	25	40	60	75	75	100
915 MHz	8	25	40	50	70	75	100

Bit Rate: 38.3kbps	Transmitter Deviation [+/- kHz]						
	30	60	90	120	150	180	210
315 MHz	don't use	30	75	100	100	100	100
433 MHz	don't use	20	50	75	100	100	100
868 MHz	don't use	10	30	40	60	75	100
915 MHz	don't use	10	25	40	60	75	75

Whenever a low frequency error is essential for the application, it is possible to "pull" the crystal to the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the "midrange", for example 16 pF. The "pull-ability" of the crystal is defined by its motional capacitance and C_0

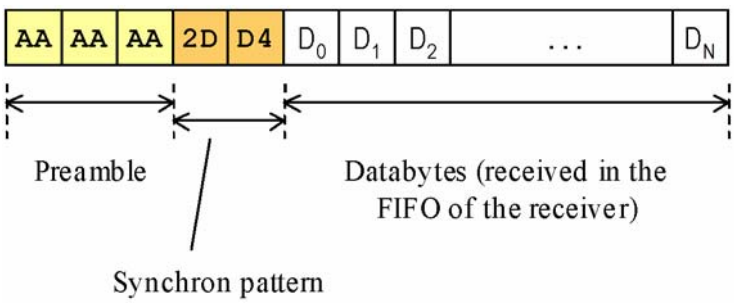
Note:

• There may be other requirements for the TX carrier accuracy with regards to the requirements as defined by standards and/or channel separations.

EXAMPLE APPLICATIONS: DATA PACKET TRANSMISSION

Data packet structure

An example data packet structure using the RF02X - RF01 pair for data transmission. This packet structure is an example of how to use the high efficiency FIFO mode at the receiver side:



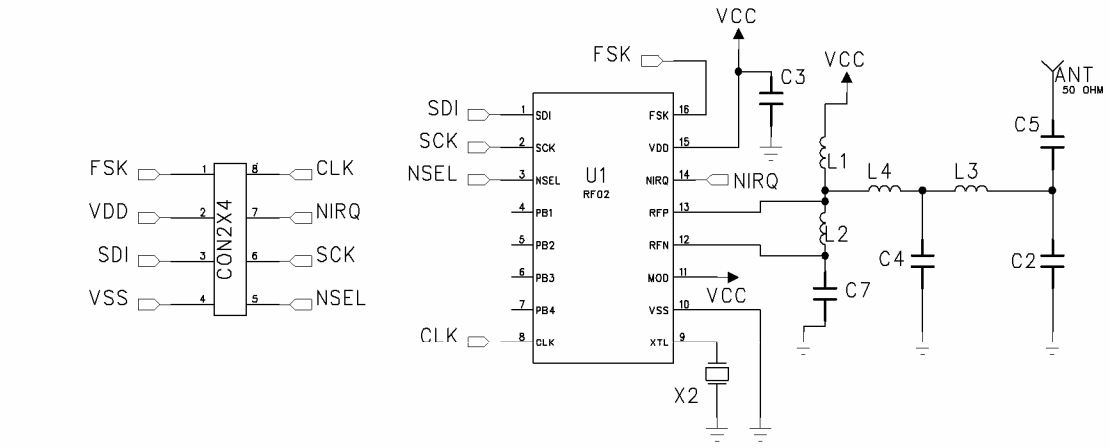
The first 3 bytes compose a 24 bit length ‘01’ pattern to let enough time for the clock recovery of the receiver to lock. The next two bytes compose a 16 bit synchron pattern which is essential for the receiver’s FIFO to find the byte synchron in the received bit stream. The synchron patters is followed by the payload. The first byte transmitted after the synchron pattern (D0 in the picture above) will be the first received byte in the FIFO.

Important: The bytes of the data stream should follow each other continuously, otherwise the clock recovery circuit of the receiver side will be unable to track.

Further details of packet structures can be found in the RF ISM-UGSB1 software development kit manual

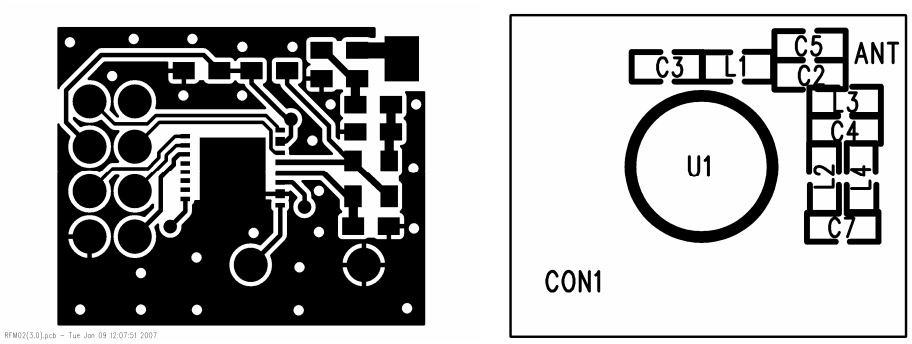
REFERENCE DESIGNS

Schematic

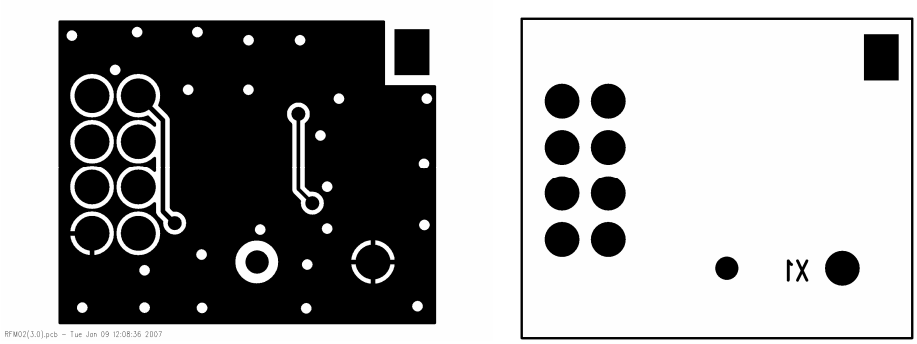


	C3	L1	L2	C7	L4	C4	L3	C2	C5
434	10nF	220nH	27nH	4.7PF	22nH	10PF	27nH	12PF	5.6PF
869	10nF	47nH	10nH	3.3PF	8.2nH	3.9PF	15nH	3.9PF	5.6PF
915	10nF	47nH	10nH	3.3PF	8.2nH	3.3PF	15nH	3.9PF	5.6PF

PCB layout



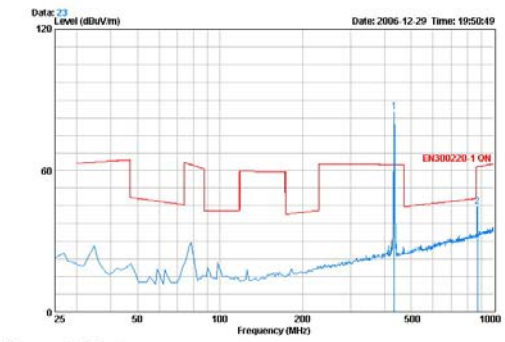
Top view



Bottom view

SGS Reports

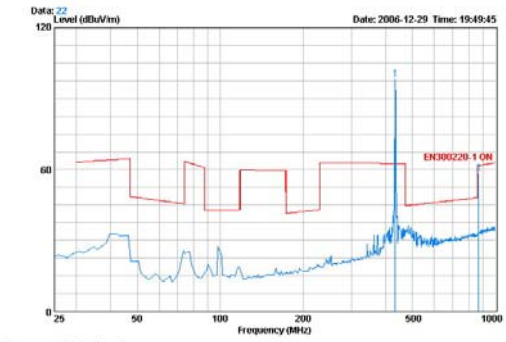
SGS



Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 HORIZONTAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	432.550	2.34	16.56	27.52	93.56	84.94	62.55	22.39
2	672.275	3.50	22.93	26.57	44.93	44.80	61.61	-16.82

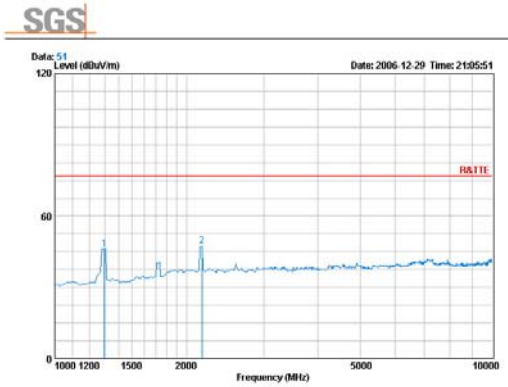
SGS



Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 VERTICAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	432.550	2.34	16.56	27.52	106.57	97.95	62.55	35.41
2	868.375	3.48	22.85	26.58	58.53	58.28	61.57	-3.29

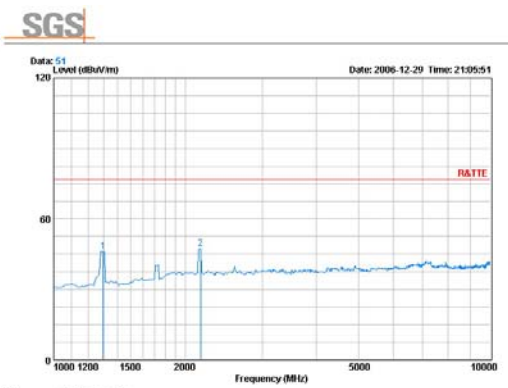
SGS



Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1	1297.000	1.28	27.66	44.76	61.95	46.13	77.00	-30.87
2 @	2170.000	1.84	32.11	44.70	58.10	47.35	77.00	-29.65

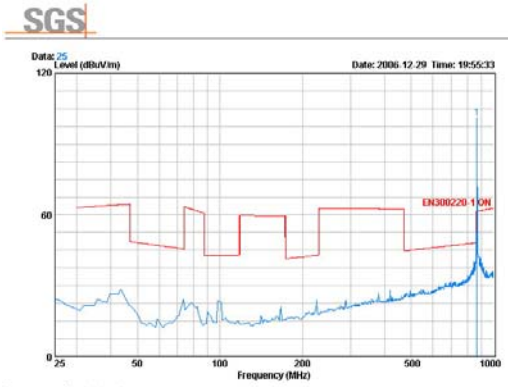
SGS



Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1	1297.000	1.28	27.66	44.76	61.95	46.13	77.00	-30.87
2 @	2170.000	1.84	32.11	44.70	58.10	47.35	77.00	-29.65

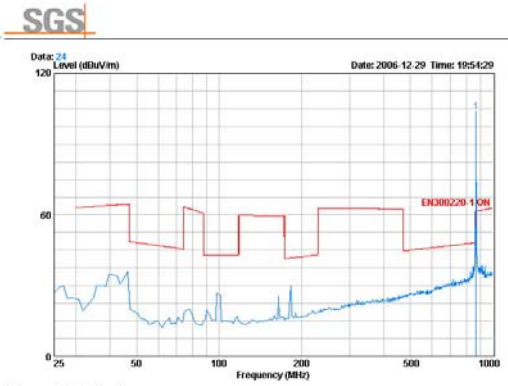
SGS



Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 HORIZONTAL
EUT : #C

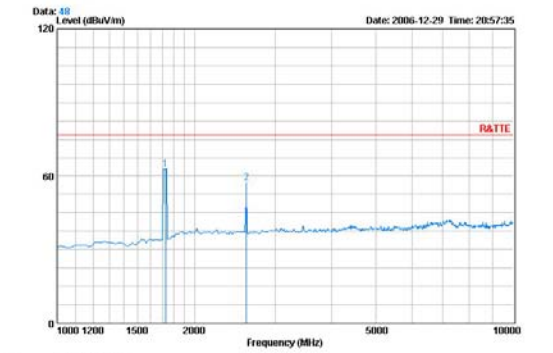
	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	868.375	3.48	22.85	26.58	101.34	101.08	61.57	39.51

SGS



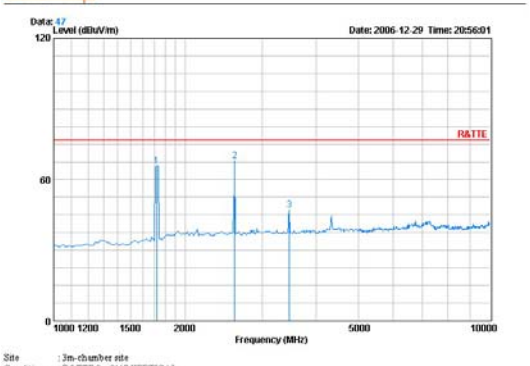
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 VERTICAL
EUT : #C

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	868.375	3.48	22.85	26.58	103.75	103.49	61.57	41.92



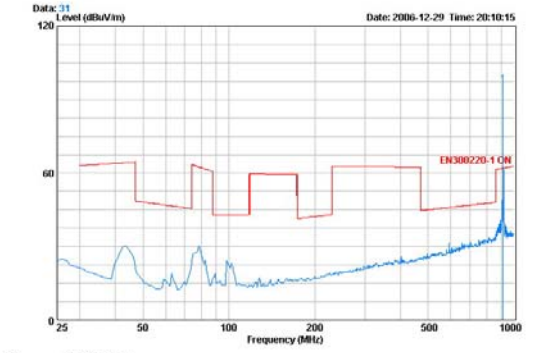
Site : 3m-chamber site
Condition : R&TTE 3m 3117 HORIZONTAL
EUT : #C

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	1729.000	1.59	29.86	44.70	76.11	62.86	77.00	-14.14
2	2602.000	2.04	32.54	44.80	67.38	57.16	77.00	-19.84



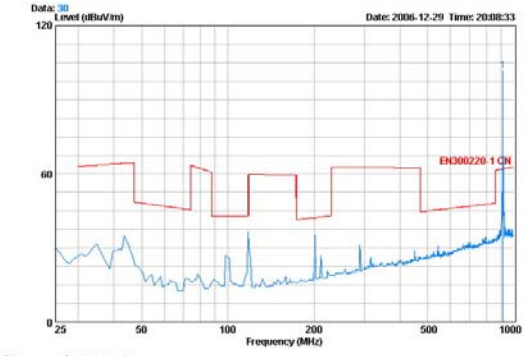
Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #C

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1	1720.000	1.59	29.82	44.70	78.87	65.58	77.00	-11.42
2 @	2602.000	2.04	32.54	44.80	70.13	67.91	77.00	-9.09
3	3466.000	2.35	33.21	45.01	56.47	47.02	77.00	-29.98



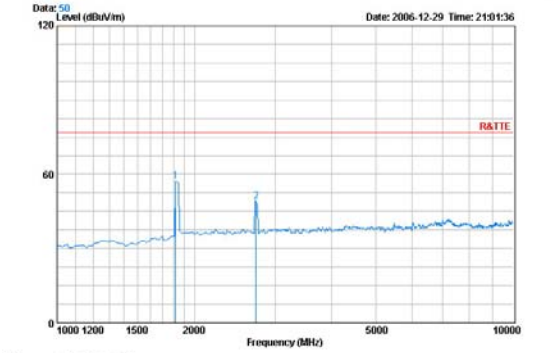
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 HORIZONTAL
EUT : #E

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	914.200	3.62	23.26	26.43	95.64	96.09	62.05	34.04



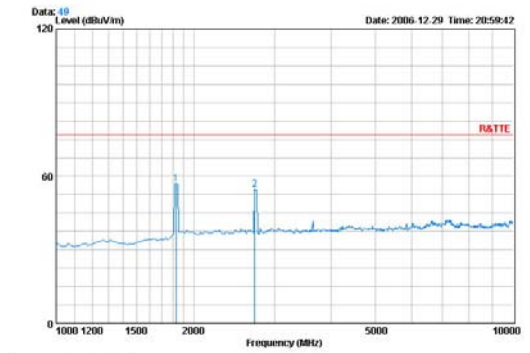
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 VERTICAL
EUT : #E

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	914.200	3.62	23.26	26.43	101.18	101.63	62.05	39.57



Site : 3m-chamber site
Condition : R&TTE 3m 3117 HORIZONTAL
EUT : #E

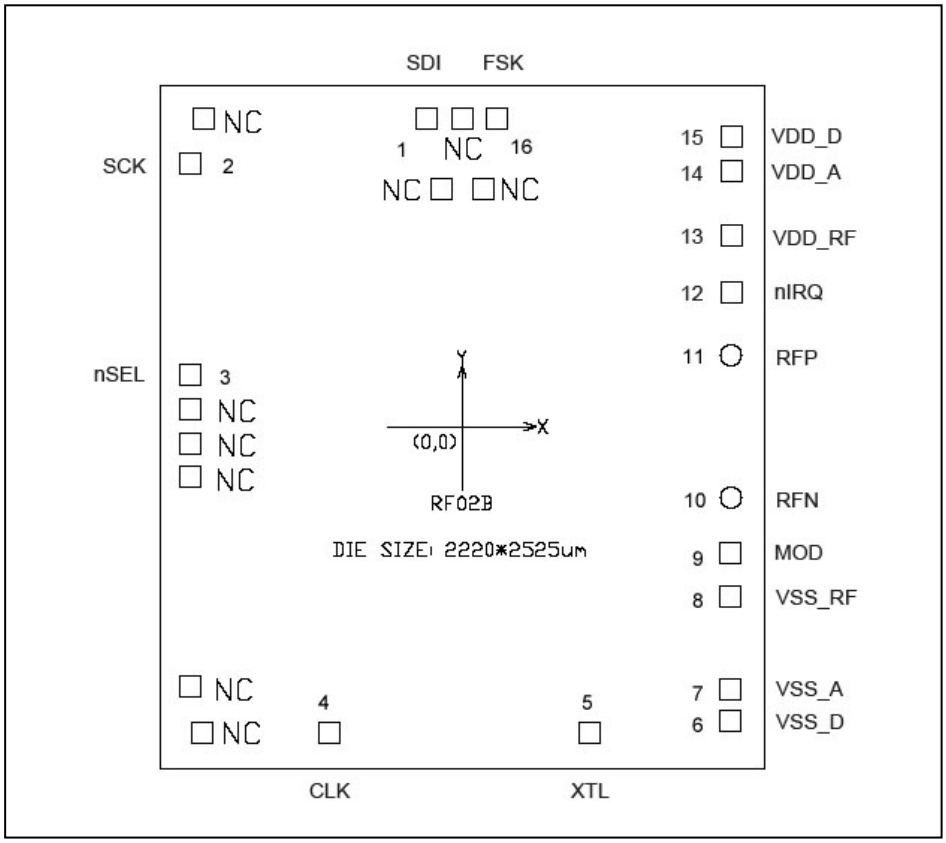
	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	1819.000	1.65	30.61	44.69	69.51	57.09	77.00	-19.91
2	2728.000	2.09	32.82	44.84	58.95	49.03	77.00	-27.97



Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #E

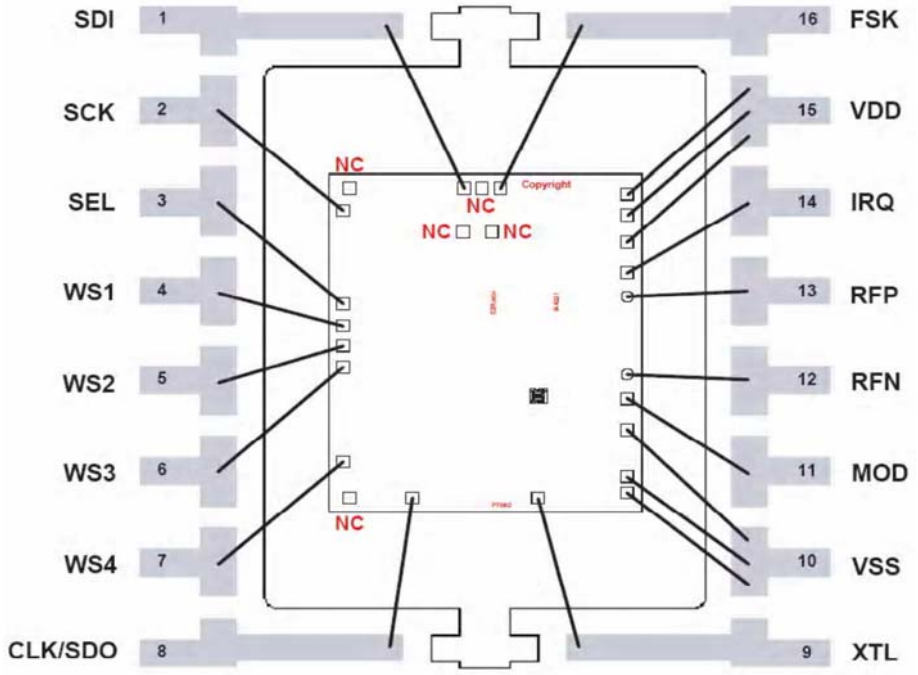
	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	1620.000	1.66	30.70	44.60	69.20	56.87	77.00	-20.13
2	2719.000	2.09	32.01	44.03	64.43	54.49	77.00	-22.51

RF02 BONDING DIAGRAM



Pad Opening: 85um square, except 76um octagon pads (AN1, AN2)

Die Size: 2220 X 2525 um



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http://www.hoperf.cn
http://hoperf.en.alibaba.com